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RTL8309M-CG

SINGLE-CHIP 9-PORT 10/100M ETHERNET SWITCH CONTROLLER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2013/06/22	First release.
1.1	2014/01/07	Revised Table 3, page 9 (pin 51 description) Revised Table 6, page 11 (pin 34, 33, and 52 descriptions)
1.2	2015/03/09	Add ACL, MAC Limit, Port Isolation, MIBS, IGMP & MLD Snooping, CPU Tag, 802.1x, 802.1D, Port Mirror Function descriptions.
1.2	2016/12/19	Revised b normal value from 0.22 to 0.20 in section 10.1 Mechanical Dimensions Notes, page 58.

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1. General Description

The RTL8309M-CG is a 9-port 10/100M Ethernet switch controller that integrates memory, nine MACs, and eight physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. It supports a (T)MII/RMII interface for external devices to connect to the 9th MAC. The external device could be a routing engine, HomePNA, HomePlug, or VDSL transceiver depending on the application. In order to accomplish diagnostics in complex network systems, the RTL8309M provides a loopback feature in each port.

The RTL8309M supports several advanced QoS functions with four-level priority queues to improve multimedia or real-time networking applications, including:

- Multi-priority assignment
- Differential queue weight
- Port-based rate limitation
- Queue-based rate limitation

For multicast applications, the RTL8309M supports IGMPv1/v2/v3 and MLDv1/v2 snooping.

To meet security and management requirements, the RTL8309M supports IEEE 802.1x Port-based/MAC-based Access Control, MAC Address Limits, Port Isolation, Port Mirroring, and also supports twelve 32-bit and two 64-bit MIB Counters on each port.

The RTL8309M supports 16 VLAN groups. These can be configured as port-based VLANs and/or 802.1Q tag-based VLANs. The RTL8309M also supports VLAN learning, with four Independent VLAN Learning (IVL) filtering databases. The RTL8309M contains a 2K-entry address lookup table. A 4-way associative hash algorithm avoids hash collisions and maintains forwarding performance.

For IGMP/MLD snooping application, each of the 2K entries can be configured as a multicast entry that indicates the matched packets will be forwarded to specific multi ports. For IEEE 802.1x application, each of the 2K entries can be configured as an authorized or unauthorized entry.

Maximum packet length is 2048 bytes. Three types of independent storm filter are provided to filter packet storms, and an intelligent switch engine prevents Head-of-Line blocking problems. The filtering function is supported for IEEE 802.1D specified reserved multicast addresses.

The RTL8309M supports Energy-Efficient Ethernet mode (EEE; defined in IEEE 802.3az) to minimize system power consumption. Energy-Efficient Ethernet (EEE) supports Low Power Idle Mode. When Low Power Idle Mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

To simplify the peripheral power circuit, the RTL8309M integrates one LDO regulator to generate 1.0V from a 3.3V input power, and needs only one external diode.

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2. Features

Basic Switching Functions

- 9-port switch controller with memory and transceiver for 10Base-T and 100Base-TX
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Complies with IEEE 802.3/802.3u auto-negotiation
- Built-in high efficiency SRAM for packet buffer, with 2K-entry lookup table and two 4-way associative hash algorithms
- 2048 byte maximum packet length
- Flow control fully supported
  - Half duplex: Back pressure flow control
  - Full duplex: IEEE 802.3x flow control
- Supports (T)MII/RMII interface connection to external MAC or PHY via 2 modes:
  - PHY mode (T)MII for router applications
  - MAC mode (T)MII for HomePNA or other PHY applications
  - RMII REFCLK output or input

Service Quality

- Supports high performance QoS function on each port
  - Supports 4-level priority queues
  - Weighted round robin service
  - Supports strict priority
  - Input/Output port bandwidth control
  - Queue-based bandwidth control
  - ACL-based, 1Q-based, Port-based, DSCP-based, IP address-based, and other types of priority assignments
- Supports IEEE 802.1p Traffic Re-marking
- Supports 16-entry ACL for advanced applications
- Supports IGMP v1/v2/v3 and MLD v1/v2 snooping

Security and Management

- Supports MAC Limit
- Supports Port Isolation
- Supports IEEE 802.1x
- Supports 32-bit and 64-bit smart counter for per port RX/TX byte/packet count, collision counter, and error counter
- Supports reserved control frame filtering
- Supports advanced storm filtering
- Supports Port Mirroring
- Supports proprietary CPU tag for traffic management
- Optional EEPROM interface for configuration

VLAN Functions

- Supports up to 16 VLAN groups
- Flexible 802.1Q port/tag-based VLAN
- Supports four IVLs
- Leaky VLAN for unicast/multicast/broadcast/ARP packets

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Power Saving Functions

- Supports Energy-Efficient Ethernet (EEE) function (IEEE 802.3az)
- Link Down Power Saving Mode

Diagnostic Functions

- Supports hardware loop detection function with LEDs and buzzer to indicate the existence of a loop
- Supports cable diagnosis (RTCT function)
- Supports IEEE 802.1D
- Flexible LED indicators
    - RTCT status indication
    - Loop status indication
    - LEDs blink upon reset for LED diagnostics

Other Features

- Optional MDI/MDIX auto crossover for plug-and-play
- Physical layer port Polarity Detection and Correction function
- Robust baseline wander correction for improved 100Base-TX performance
- 25MHz crystal or 3.3V OSC input
- Single 3.3V power input can be transformed by integrating an LDO regulator to generate 1.0V from 3.3V via a low-cost external Diode
- Low power, 1.0/3.3V, 55nm CMOS technology
- 88-pin QFN 'Green' package

3. System Applications

- 9-port switch (10Base-T & 100Base-TX)
- xDSL/cable modem router or home gateway applications
- HomePNA/HomePlug bridge solutions
- Set-top box/TV

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4. Block Diagram

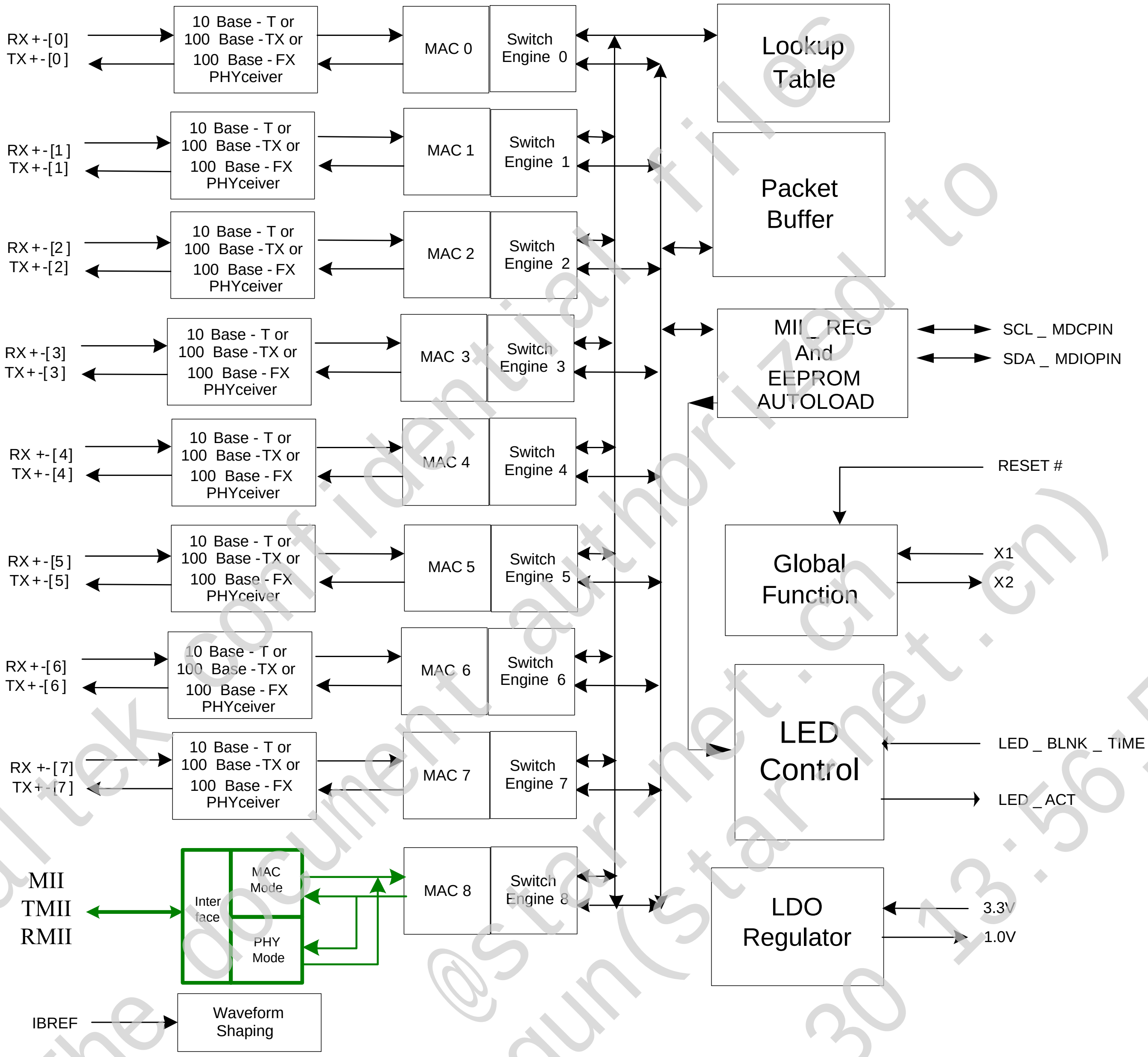

Figure 1. Block Diagram

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5. Pin Assignments

5.1. Pin Assignments Diagram

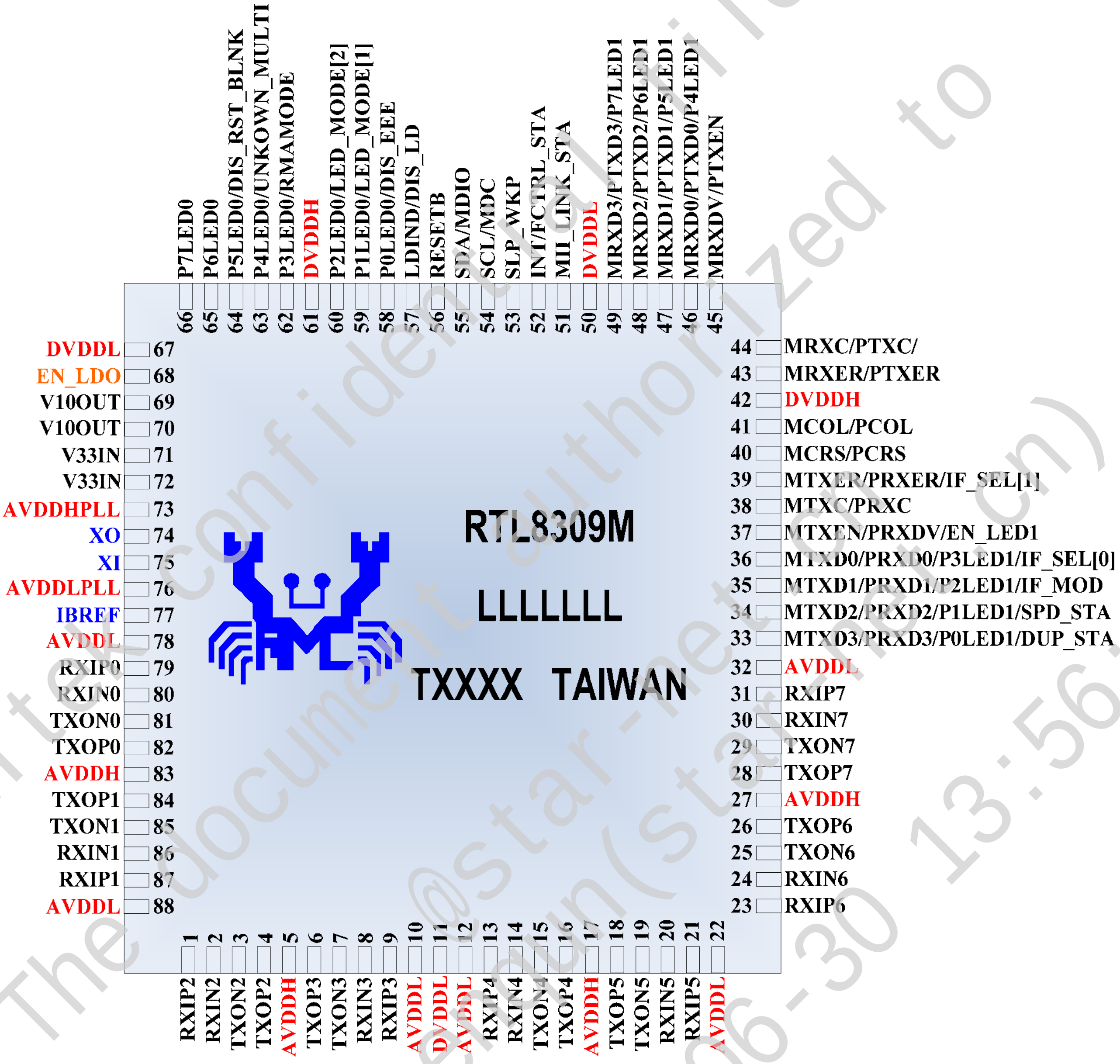

Figure 2. Pin Assignments

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5.2. Package Identification

Green package is indicated by a 'G' in the location marked 'TXXXX' in Figure 2.

5.3. Pin Assignments Table

'Type' codes used in the following table: A=Analog, D=Digital, I=Input, O=Output, I/O=Input/Output, I_{PU}=Input Pin with Pull-Up Resistor, I_{PD}=Input Pin with Pull-Down Resistor.

Table 1. Pin Assignments Table

Name	Pin No.	Type	Name	Pin No.	Type
RXIP[2]	1	AI/O	MCRS	40	I/O_{PD}
RXIN[2]	2	AI/O	MCOL	41	I/O_{PD}
TXON[2]	3	AI/O	DVDDH	42	P
TXOP[2]	4	AI/O	MRXER	43	I_{PD}
AVDDH	5	AP	MRXC	44	I/O_{PD}
TXOP[3]	6	AI/O	MRXDV	45	I_{PD}
TXON[3]	7	AI/O	MRXD0	46	I/O_{PD}
RXIN[3]	8	AI/O	MRXD1	47	I/O_{PD}
RXIP[3]	9	AI/O	MRXD2	48	I/O_{PD}
AVDDL	10	AP	MRXD3	49	I/O_{PD}
DVDDL	11	P	DVDDL	50	P
AVDDL	12	AP	MII_LINK_STA	51	I_{PD}
RXIP[4]	13	AI/O	INT	52	I/O_{PU}
RXIN[4]	14	AI/O	SLP_WKP	53	O_{PU}
TXON[4]	15	AI/O	SCL/MDC	54	I/O_{PU}
TXOP[4]	16	AI/O	SDA/MDIO	55	I/O_{PU}
AVDDH	17	AP	RESETB	56	I_{PU}
TXOP[5]	18	AI/O	LDIND	57	I/O_{PU}
TXON[5]	19	AI/O	P0LED0	58	I/O_{PD}
RXIN[5]	20	AI/O	P1LED0	59	I/O_{PD}
RXIP[5]	21	AI/O	P2LED0	60	I/O_{PD}
AVDDL	22	AP	DVDDH	61	P
RXIP[6]	23	AI/O	P3LED0	62	I/O_{PD}
RXIN[6]	24	AI/O	P4LED0	63	I/O_{PD}
TXON[6]	25	AI/O	P5LED0	64	I/O_{PD}
TXOP[6]	26	AI/O	P6LED0	65	I/O_{PD}
AVDDH	27	AP	P7LED0	66	I/O_{PD}
TXOP[7]	28	AI/O	DVDDL	67	P
TXON[7]	29	AI/O	EN_LDO	68	AI
RXIN[7]	30	AI/O	V10OUT	69	AO
RXIP[7]	31	AI/O	V10OUT	70	AO
AVDDL	32	AP	V33IN	71	AP
MTXD3	33	I/O_{PD}	V33IN	72	AP
MTXD2	34	I/O_{PD}	AVDDHPLL	73	AP
MTXD1	35	I/O_{PD}	XO	74	O
MTXD0	36	I/O_{PD}	XI	75	I
MTXEN	37	I/O_{PD}	AVDDLPLL	76	AP
MTXC	38	I/O_{PD}	IBREF	77	AO
MTXER	39	I/O_{PD}	AVDDL	78	AP

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Name	Pin No.	Type
RXIP[0]	79	AI/O
RXIN[0]	80	AI/O
TXON[0]	81	AI/O
TXOP[0]	82	AI/O
AVDDH	83	AP
TXOP[1]	84	AI/O
TXON[1]	85	AI/O
RXIN[1]	86	AI/O
RXIP[1]	87	AI/O
AVDDL	88	AP
E-PAD	E-PAD	G

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6. Pin Descriptions

6.1. Pin Assignment Codes

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value is about 75KΩ)

I_{PD}: Input Pin With Pull-Down Resistor; (Typical Value is about 75KΩ)

I/O_{PU}: I_{PU} and O_{PU}

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value is about 75KΩ)

O_{PD}: Output Pin With Pull-Down Resistor; (Typical Value is about 75KΩ)

I/O_{PD}: I_{PD} and O_{PD}

6.2. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RXIP7/RXIN7 RXIP6/RXIN6 RXIP5/RXIN5 RXIP4/RXIN4 RXIP3/RXIN3 RXIP2/RXIN2 RXIP1/RXIN1 RXIP0/RXIN0	31, 30 23, 24 21, 20 13, 14 9, 8 1, 2 87, 86 79, 80	AI/O	-	Differential Receive Data Input. Port0-7 support 10Base-T, 100Base-TX.
TXOP7/TXON7 TXOP6/TXON6 TXOP5/TXON5 TXOP4/TXON4 TXOP3/TXON3 TXOP2/TXON2 TXOP1/TXON1 TXOP0/TXON0	28, 29 26, 25 18, 19 16, 15 6, 7 4, 3 84, 85 82, 81	AI/O	-	Differential Transmit Data Output. Port0-7 support 10Base-T, 100Base-TX.

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6.3. (T)MII/RMII Port MAC Interface Pins

Table 3. (T)MII/RMII Port MAC Interface Pins

Pin Name	Pin No.	Type	Description	Default

MRXD[3:0] /PTXD[3:0]	49, 48, 47, 46	I/O_{PD}	For (T)MII MAC mode, these pins are MRXD[3:0], (T)MII receive data nibble.
			For (T)MII PHY mode, these pins are PTXD[3:0], (T)MII transmit data nibble.
			For RMII mode, pins MRXD[3:2] is not used.
				-

MRXDV/PTXEN	45	I_{PD}	For (T)MII MAC mode, this pin represents MRXDV, (T)MII receive data valid.
			For (T)MII PHY mode, this pin represents PTXEN, (T)MII transmit enable.
			For RMII mode, this pin is used as CRS_DV.
				-

MRXC/PTXC	44	I/O_{PD}	For (T)MII MAC mode, this pin represents MRXC, (T)MII receive clock (acts as input).
			For (T)MII PHY mode, this pin represents PTXC, (T)MII transmit clock (acts as output).
			For MII mode, this pin is 25MHz for 100Mbps and 2.5MHz for 10Mbps.
			For TMII mode, this pin is 50MHz for 200Mbps and 5MHz for 20Mbps.
			For RMII mode, this pin is used as REFCLK output or input based on configuration.
				-

MRXER/PTXER	43	I_{PD}	For MII MAC mode, this pin represents MRXER, MII receive error. For MII PHY mode, this pin represents PTXER, MII transmit error. For TMII and RMII mode, this pin is not used.	-
MTXER/PRXER	39	I/O_{PD}	For MII MAC mode, this pin represent MTXER, MII transmit error For MII PHY mode, this pin represent PRXER, MII receive error For TMII and RMII mode, this pin is not used.	
MCOL/PCOL	41	I/O_{PD}	For MII MAC mode, this pin represents MCOL, MII collision detect (acts as input). For MII PHY mode, this pin represents PCOL, MII collision detect (acts as output). For TMII and RMII mode, this pin is not used.	-
MCRS/PCRS	40	I/O_{PD}	For MII MAC mode, this pin represents MCRS, MII collision detect (acts as input). For MII PHY mode, this pin represents PCRS, MII collision detect (acts as output). For TMII and RMII mode, this pin is not used.	-

MTXD[3:0] /PRXD[3:0]	33, 34, 35, 36	I/O_{PD}	Output After Reset.
			For (T)MII MAC mode, these pins are MTXD[3:0], (T)MII transmit data of MAC.
			For (T)MII PHY mode, these pins are PRXD[3:0], (T)MII receive data of MAC.
			For RMII mode, pins MTXD[3:2] is not used.
				-

MTXEN/PRXDV	37	I/O_{PD}	For (T)MII MAC mode, this pin represents MTXEN, (T)MII transmit enable.
			For (T)MII PHY mode, this pin represents PRXDV, (T)MII receive data valid.
			For RMII mode, this pin is used as TXEN
				-

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Pin Name	Pin No.	Type	Description	Default

MTXC/PRXC	38	I/O_{PD}	For (T)MII MAC mode, this pin represents MTXC, (T)MII transmit clock (acts as input).
			For (T)MII PHY mode, this pin represents MRXC, (T)MII receive clock (acts as output).
			For MII mode, this pin is 25MHz for 100Mbps and 2.5MHz for 10Mbps.
			For TMII mode, this pin is 50MHz for 200Mbps and 5MHz for 20Mbps.
			For RMII mode, this pin is not used.
				-

MII_LNK_STA	51	I_{PD}	Provides (T)MII/RMII port (9th port) Link Status for MAC module at (T)MII/RMII MAC/PHY operation mode in real time. This pin sets the link status of the (T)MII/RMII port MAC module in real-time. 0: MAC8 is link down 1: MAC8 is link up	0

6.4. Miscellaneous Pins

As the output of the RTL8309M is 3.3V, the serial EEPROM and external device must be 3.3V compatible.

Table 4. Miscellaneous Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LDIND	57	I/O_{PU}	10	Loop Indication Used by LED and Buzzer.
INT	52	I/O_{PU}	4	Setting any flag bit in the interrupt event flag register will cause this pin to be pulled low and output logical '0'. Only when all flag bits in the interrupt event flag register are cleared, this pin will be pulled high and output logical '1'.
SLP_WKP	53	O_{PU}	4	This pin is used to power off the CPU for power saving. It is also used to power on or wake up the CPU when a wakeup event occurs.
SCL/MDC	54	I/O_{PU}	4	I2C Interface Clock for EEPROM Auto Load when Power On. After power on, this pin is MDC/MDIO Interface Clock for access registers.
SDA/MDIO	55	I/O_{PU}	4	I2C Interface Data Input/Output for EEPROM Auto Load when Power On. After power on, this pin is MDC/MDIO Interface Data Input/Output for access registers.
RESETB	56	I_{PU}	-	System Pin Reset Input.
XI	75	AI	-	25MHz Crystal Clock Input. The clock tolerance is ±50ppm.
XO	74	AO	-	25MHz Crystal Clock Output Pin. When the pin of XI is using an oscillator this pin should be floating.
IBREF	77	AO	-	Reference Resistor for PHY Bandgap. A 2.49KΩ (1%) resistor should be connected between IBREF and GND.

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6.5. Port LED Pins

All LED statuses are represented as active-low or high depending on input strapping.

Those pins that are dual-function pins are output for LED, or input for strapping. Below are LED descriptions only.

Table 5. Port LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0LED0	58	I/O_{PD}	10	LED0 for Port0 Status Indication.
P1LED0	59	I/O_{PD}	10	LED0 for Port1 Status Indication.
P2 LED0	60	I/O_{PD}	10	LED0 for Port2 Status Indication.
P3 LED0	62	I/O_{PD}	10	LED0 for Port3 Status Indication.
P4 LED0	63	I/O_{PD}	10	LED0 for Port4 Status Indication.
P5 LED0	64	I/O_{PD}	10	LED0 for Port5 Status Indication.
P6 LED0	65	O_{PD}	10	LED0 for Port6 Status Indication.
P7 LED0	66	O_{PD}	10	LED0 for Port7 Status Indication.
P0LED1 (MTXD3)	33	I/O_{PD}	10	LED1 for Port0 Status Indication.
P1LED1 (MTXD2)	34	I/O_{PD}	10	LED1 for Port1 Status Indication.
P2 LED1 (MTXD1)	35	I/O_{PD}	10	LED1 for Port2 Status Indication.
P3 LED1 (MTXD0)	36	I/O_{PD}	10	LED1 for Port3 Status Indication.
P4 LED1 (MRXD0)	46	I/O_{PD}	10	LED1 for Port4 Status Indication.
P5 LED1 (MRXD1)	47	I/O_{PD}	10	LED1 for Port5 Status Indication.
P6 LED1 (MRXD2)	48	I/O_{PD}	10	LED1 for Port6 Status Indication.
P7 LED1 (MRXD3)	49	I/O_{PD}	10	LED1 for Port7 Status Indication.

6.6. Strapping Pins

Pins that are dual function pins are outputs for LED or inputs for strapping. Below are strapping descriptions only.

Table 6. Strapping Pins

Pin Name	Pin No.	Type	Default	Description
DISLD (LDIND)	57	I/O_{PU}	-	Disable Loop Detection Function. 0: Enable 1: Disable (default)
DIS_EEE (P0LED0)	58	I/O_{PD}	-	Disable EEE Function. 0: Enable EEE function (default) 1: Disable EEE function

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Pin Name	Pin No.	Type	Default	Description
LED_MODE1 (P1LED0)	59	I/O_{PD}	-	LED Mode[2:1] Select. 2'b00/2'b01: Mode 0/1: Link+Act (default) 2'b10: Mode 2: Duplex 2'b11: Mode 3: Speed100+Act
LED_MODE2 (P2LED0)	60	I/O_{PD}	-	LED Mode[2:1] Select. 2'b00/2'b01: Mode 0/1: Link+Act (default) 2'b10: Mode 2: Duplex 2'b11: Mode 3: Speed100+Act
RMAMODE (P3LED0)	62	I/O_{PD}	-	RMA Mode Select. 0: Mode0 is selected (default) 01-80-c2-00-00-02 is drop and 01-80-c2-00-00-11 ~ 01-80-c2-00-00-1F, 01-80-c2-00-00-21 packets are forwarded. 1: Mode1 is selected 01-80-c2-00-00-02 is forward and 01-80-c2-00-00-11 ~ 01-80-c2-00-00-1F, 01-80-c2-00-00-21 packets are dropped.
UNKOWN_MULTI (P4LED0)	63	I/O_{PD}	-	Enable Unknown Multicast Data Packet Drop. 0: Forward all unknown multicast data packet (default) 1: Drop all unknown multicast data packet (except IGMP/MLD and RMA packet)
DIS_RST_BLNK (P5LED0)	64	I/O_{PD}	-	Disable LED Power on Blinking. 0: Enable (default) 1: Disable
IF_MODE (MTXD1)	35	I/O_{PD}	-	MAC8 Interface Mode. 0: MAC mode(default) 1: PHY mode
IF_SEL[0] (MTXD0)	36	I/O_{PD}	-	MAC8 Interface Select. 00: Disable MAC8 interface(default) 01: MII interface 10: TMII interface 11: RMII interface
IF_SEL[1] (MTXER)	39	I/O_{PD}	-	MAC8 Interface Select. 00: Disable MAC8 interface(default) 01: MII interface 10: TMII interface 11: RMII interface
EN_LED1 (MTXEN)	37	I/O_{PD}	-	Enable LED1 group. 0: Disable LED1, LED1 pin used as MAC8 interface 1: Enable LED1
SPD_STA (MTXD2)	34	I/O_{PD}	-	Force MAC8 Speed. 0: MAC8 is 10Mbps 1: MAC8 is 100Mbps,
DUP_STA (MTXD3)	33	I/O_{PD}	-	Force MAC8 Duplex. 0: MAC8 is half duplex 1: MAC8 is full duplex
FCTRL_STA (INT)	52	I/O_{PU}	-	Force MAC8 Flow Control. 0: MAC8 is disabled 1: MAC8 is enabled

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6.7. LDO Pins

Table 7. LDO Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
V10OUT	69,70	AO	-	LDO 1.0V Output.
V33IN	71,72	AP	-	LDO 3.3V Input.
EN_LDO	68	AI	-	LDO Enable. 0: Disable 1: Enable (default)

6.8. Power and GND Pins

Table 8. Power and GND Pins

Pin Name	Pin No.	Type	Description
AVDDH	5, 17, 27, 83	AP	Analog Power 3.3V.
AVDDL	10, 12, 22, 32, 78, 88	AP	Analog Power 1.0V.
AVDDHPLL	73	AP	Power 3.3V for PLL.
AVDDLPLL	76	AP	Power 1.0V for PLL.
DVDDH	42, 61	P	Digital Power 3.3V for IO Pin.
DVDDL	11, 50, 67	P	Digital Power 1.0V for Core Voltage.
GND	E-PAD	G	Ground for Whole Chip.

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7. Basic Functional Description

7.1. *Switch Core Function Overview*

7.1.1. Flow Control

The RTL8309M supports IEEE 802.3x full duplex flow control, force mode full duplex flow control, and optional half duplex backpressure.

7.1.1.1 IEEE 802.3x Full Duplex Flow Control

For UTP with auto-negotiation ability, the pause ability of full duplex flow control is enabled by internal registers via SMI on a per-port basis after reset. IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8309M. If the auto-negotiation result of the IEEE 802.3x pause ability is 'Enabled', the full duplex 802.3x flow control function is enabled. Otherwise, the full duplex IEEE 802.3x flow control function is disabled.

7.1.1.2 Half Duplex Back Pressure

There are two mechanisms for half duplex backpressure; collision-based or carrier-based.

Collision-Based Backpressure (Jam Mode)

If the buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- The RTL8309M will drive TXEN to high and send the preamble; SFD and a 4-byte Jam signal (pattern is 0xAA). The RTL8309M will then drive TXEN to low
- When the link partner receives the Jam signal, it will feedback a 4-byte signal (pattern is CRC^0x01), it will then drive RXDV to low
- The link partner waits for a random back-off time then re-sends the packet. The timing is shown in Figure 3

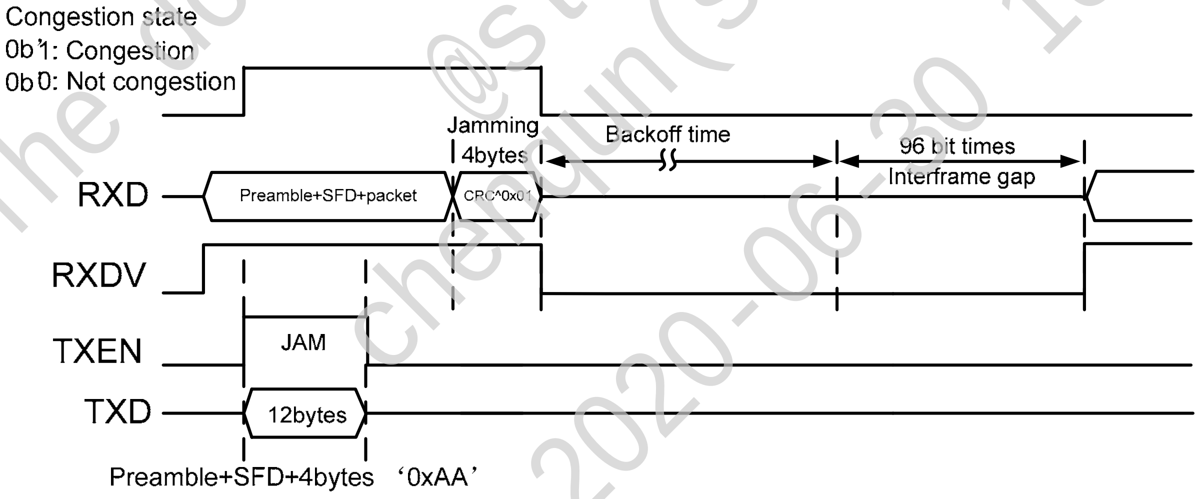

Figure 3. Collision-Based Backpressure Signal Timing

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Carrier-Based Backpressure (Defer Mode)

If the buffer is about to overflow, this mechanism will send an 0xAA pattern to defer the other station's transmission. The RTL8309M will continuously send the defer signal until the buffer overflow is resolved.

7.1.2. Address Search, Learning, and Aging

When a packet is received, the RTL8309M will use the destination MAC address and FID to index the 2048-entry lookup table. If the indexed entry is valid, the received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8309M will broadcast the packet. This is the 'Address Search'.

The RTL8309M then combines the source MAC address and the FID to index the 2048-entry lookup table. If the entry is not in the table it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information when LRU is enabled. This is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The lookup engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged-out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8309M is between 200 and 400 seconds.

7.1.3. Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. A controlled randomization process called 'truncated binary exponential backoff' determines the scheduling of the retransmissions. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k = min (n, backoffLimit). IEEE 802.3 defines the backoffLimit as 10.

7.1.4. InterFrame Gap

The InterFrame Gap is 9.6µs for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

7.1.5. Illegal Frame

Illegal frames such as CRC error packets, runt packets (length < 64 bytes), and oversize packets (length > maximum length), will be discarded.

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7.2. *Physical Layer Functional Overview*

7.2.1. Auto-Negotiation

The RTL8309M obtains the states of duplex, speed, and flow control ability for each port through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8309M advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability. The RTL8309M also advertises the Energy Efficient Ethernet (EEE) capability to the link partner.

7.2.2. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.2.3. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.2.4. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

7.2.5. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects are significantly reduced.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which further reduces EMI emissions.

7.2.6. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

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7.2.7. Power-Down Mode

The RTL8309M implements power-down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8309M to enter power-down mode. This disables all transmit/receive functions, except SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface).

7.2.8. Crossover Detection and Auto Correction

During the link setup phase, the RTL8309M checks whether it receives active signals on every port in order to determine if a connection can be established. In cases where the receiver data pin pair is connected to the transmitter data pin pair of the peer device and vice versa, the RTL8309M automatically changes its configuration and swaps receiver/transmitter data pins as required. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8309M will reconfigure the port to ensure proper connection. This replaces the DIP switch commonly used for reconfiguring a port on a hub or switch.

Note: IEEE 802.3 compliant forced mode 100M ports with Autoxover have link problems with NWay (Auto-Negotiation) ports. It is recommended to not use Autoxover for forced 100M.

7.2.9. Polarity Detection and Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted-pair cable is transmitted in differential form. That is, the signal is transmitted on two wires in each direction with inverse polarities (+/-). If wiring on the connector is faulty, or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8309M operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8309M is operating in 100Base-TX mode.

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7.3. General Function Overview

7.3.1. Power-On Sequence

Two power voltage types are required for RTL8309M normal operation, 3.3V and 1.0V. The 1.0V is converted from 3.3V via the LDO of the RTL8309M.

- Ta is the moment when 3.3V power is higher than 2.6V (±5%). 3.3V power never falls lower than 2.6V (±5%) after Ta
- Tb is the moment when 1.0V power is higher than 0.71V (±10%). 1.0V power never falls lower than 0.71V (±10%) after Tb
- Tc is the moment when both 3.3V and 1.0V power are stable (the voltage is always in the legal operating range)
- Td is the moment that the pin reset signal is de-asserted
- Te is the moment that the RTL8309M device is ready to be accessed by an external CPU

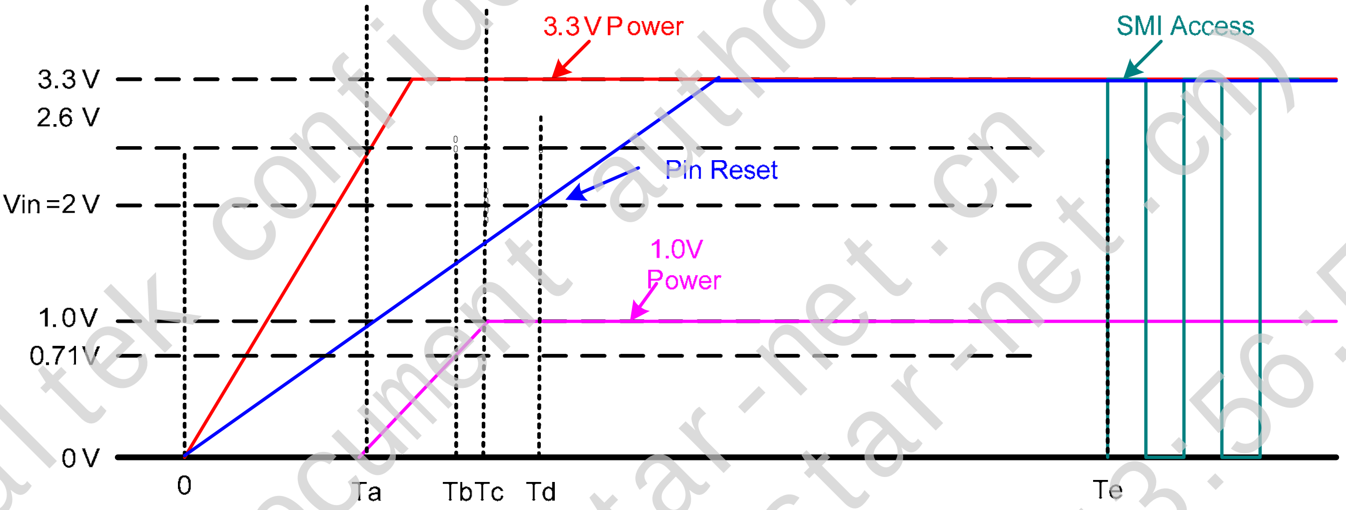

Figure 4. Power-On Sequence

The requirements are:

- The time of Ta should be between 500µs and 20ms
- The sequence of Ta is always less than Tb for the LDO of the RTL8309M. In principle, the sequence of Td and Ta/Tb/Tc is also not required. The sequence of Td > 5ms is recommended
- The time from Te to the later of Ta/Tb/Td is the sum of the time of the EEPROM loading + 30ms. The EEPROM loading time varies according to the autoloaded data bytes in the serial EEPROM
- Reset

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Depending on the type of reset, the whole or just part of the RTL8309M is initialized. There are several ways to reset the RTL8309M.

- Hardware reset for the whole chip via pin RESET# or power-on
- Soft reset for packet buffer, queue, and MIB counter via register SoftReset
- PHY software reset for each PHY by register reset

Hardware Reset: Power-on, or pull the RESET# pin low for at least 1µs. The RTL8309M resets the whole chip and after all power is ready and the RESET# pin is de-asserted, it gets initial values from pins and serial EEPROM.

Soft Reset: The RTL8309M does not reset the LUT, LED circuit, and all registers, and does not load data from serial EEPROM and pins to registers. The packet buffer, queue, and MIB counter will be reset. After changing the queue number via SMI (Serial Management Interface), the external device must perform a soft reset in order to update the configuration.

PHY Software Reset: Write bit15 of Reg0 of a PHY as 1. The RTL8309M will then reset this PHY.

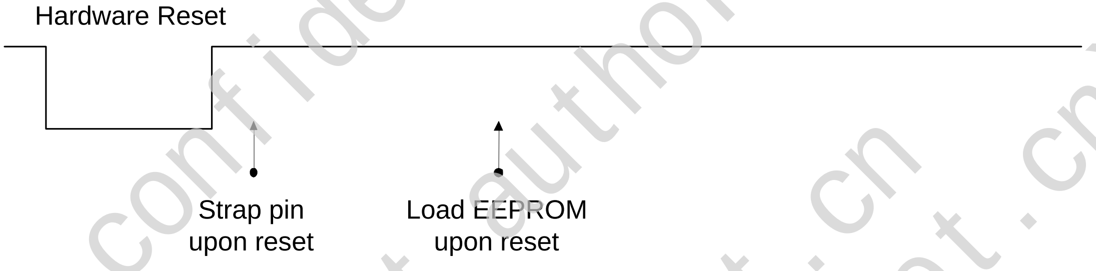

Figure 5. Reset

Some setting values for operation modes are latched from those corresponding mode pins upon hardware reset. 'Upon reset' is defined as a short time after the end of a hardware reset. Other advanced configuration parameters may be latched from serial EEPROM.

7.3.2. Setup and Configuration

The RTL8309M can be configured easily and flexibly by:

- Hardware pins upon reset
- Optional serial EEPROM upon reset (contact Realtek for detailed EEPROM configuration settings)
- Internal registers (including PHY registers for each port and global MAC registers) accessed via SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface)

There are three methods of configuration:

- Only hardware pins for normal switch applications
- Hardware pins and serial EEPROM for advanced switch applications
- Hardware pins and internal registers via SMI for applications with processor

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Two types of pins, each with internal pull-high or pull-low resistors, are used for configuration:

- Input/Output pins used for strapping upon reset and used as output pins after reset
- Input/Output pins used for strapping upon reset and used as LED indicator pins after reset. The LED statuses are represented as active-low or high depending on input strapping

Pins with default value=0 are internal pull-low and use I/O pads. They can be left floating to set the input value as low, but should not be connected to VDD without a pull-high resistor.

The serial EEPROM shares two pins, SCL/MDC and SDA/MDIO, with SMI, and is optional for advanced configuration. SCL/MDC and SDA/MDIO are tri-state during hardware reset (pin RESET#=0). The RTL8309M will try to automatically find the serial EEPROM upon reset.

Internal registers can still be accessed after reset via SMI (pin SCL/MDC and SDA/MDIO). Serial EEPROM signals and SMI signals must not exist at the same time.

7.3.3. Serial EEPROM Example

Both the 24LC01/02/04/08/16 and 24C01/02/04/08/16 can be used with the RTL8309M. The interface is a 2-wire serial EEPROM interface providing 1K/2K/4K/8K/16K bits of storage space. The EEPROM must be 3.3V compatible.

7.3.3.1 EEPROM Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below. The SCL frequency is 200 kHz.

Start Condition

A high-to-low transition of SDA with SCL high is the start condition and must precede any other command.

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge

All addresses and data are transmitted serially to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Random Read

A random read requires a 'dummy' byte write sequence to load in the data word address.

Sequential Read

For the RTL8309M, the sequential reads are initiated by a random address read. After the EEPROM receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and clock out sequential data words in series.

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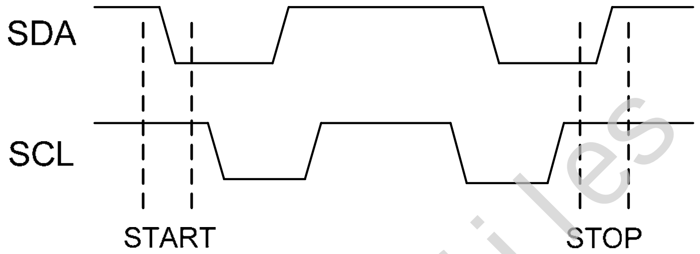

Figure 6. Start and Stop Definition

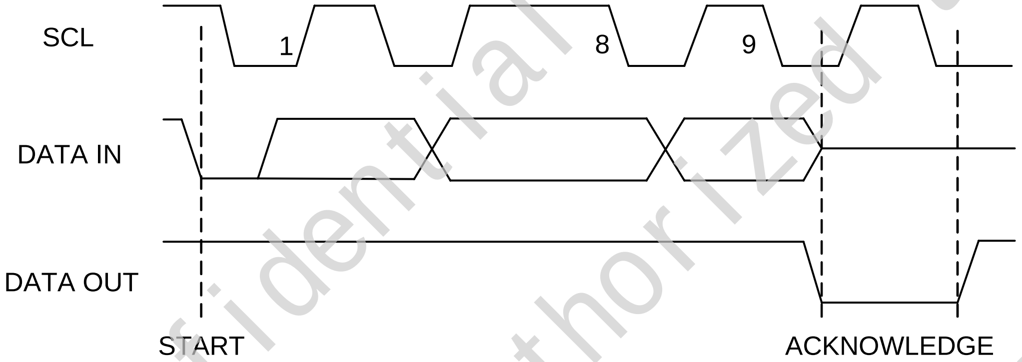

Figure 7. Output Acknowledge

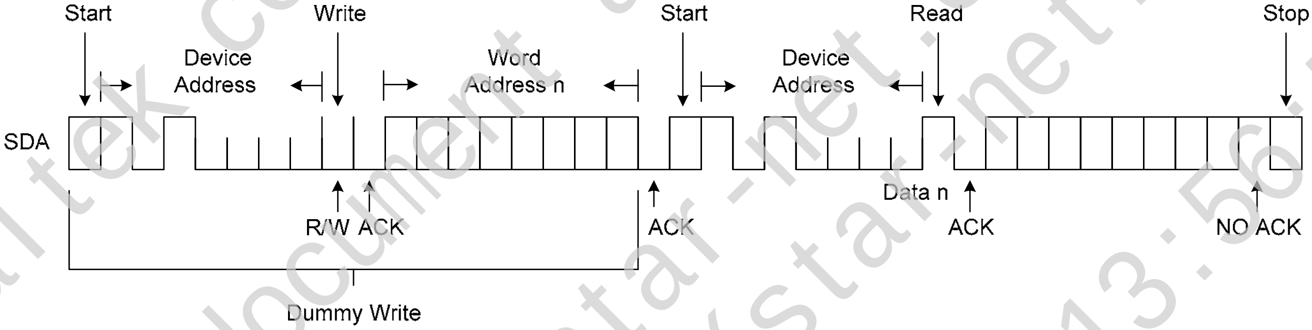

Figure 8. Random Read

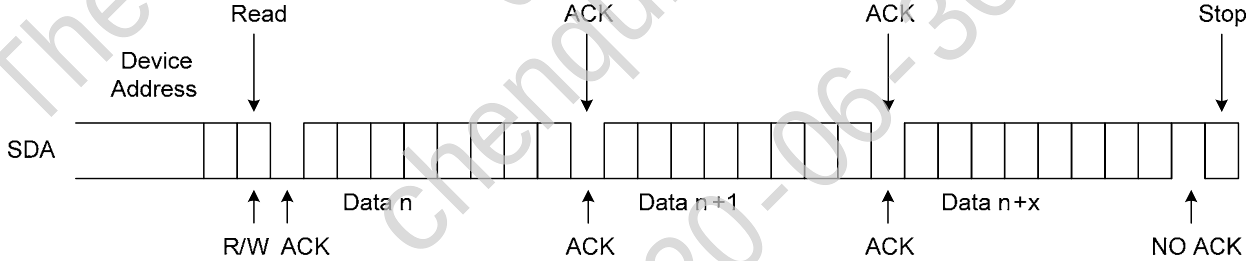

Figure 9. Sequential Read

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7.3.3.2 EEPROM Size Selection

The RTL8309M supports five serial EEPROM sizes —1k bits, 2k bits, 4k bits, 8k bits and 16k bits. Via the auto-download operation, the RTL8309M decides the size of the data downloaded to the RTL8309M from the EEPROM according to the value of the 2nd byte data in the serial EEPROM.

If the 2nd byte data = 0x01, 0x02, 0x04, 0x08 or 0x16, it means the data size is 1k bits, 2k bits, 4k bits, 8k bits or 16k bits respectively. The value of the 2nd byte should accord with the actual EEPROM data size. For example, the value of the 2nd byte cannot be '0x02' when the 24(L)C02 is used.

7.3.4. SMI

The SMI (Serial Management Interface) is also known as the MII Management Interface, and consists of two signals (MDIO and MDC). It allows external devices with SMI master mode (MDC is output) to control the state of the PHY and internal registers (SMI slave mode: MDC is input). MDC is an input clock for the RTL8309M to latch MDIO on its rising edge. The clock can run from DC to 2.5MHz. MDIO is a bi-directional connection used to write data to, or read data from the RTL8309M. The PHY address is from 0 to 7.

Table 9. Basic SMI Read/Write Cycles

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	Z0	D_{15}……D_0	Z*
Write	1……..1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	10	D_{15}……D_0	Z*

**: High-impedance. During idle time MDIO state is determined by an external 1.5KΩ pull-up resistor.*

For MDIO Manageable Device (MMD) access, the RTL8309M supports the extended SMI format.

Table 10. Extended SMI Management Frame Format

Frame	PRE	ST	OP	PHYAD	DEVAD	TA	DATA	IDLE
Address	1…1	00	00	AAAAA	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1…1	00	01	AAAAA	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1…1	00	11	AAAAA	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-Read-Increment-Address	1…1	00	10	AAAAA	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

To guarantee the first successful SMI transaction after power-on reset, the external device should delay a few moments before issuing the first SMI Read/Write Cycle relative to the rising edge of reset.

7.3.5. (T)MII/RMII Port (The 9th Port)

The RTL8309M is an 8-port Fast Ethernet switch with one extra (T)MII/RMII port for specific applications. It integrates embedded SRAM for packet storage, nine MACs, and eight physical layer transceivers for 10Base-T and 100Base-TX, into a single chip.

7.3.5.1 PHY Mode (T)MII

PHY mode (T)MII means (T)MII at the RTL8309M drives the transmitting and receiving reference clock. Figure 10 shows the signal diagram for PHY mode (T)MII. PTXER/PRXER/PCOL/PCRS are not connected in TMII PHY mode.

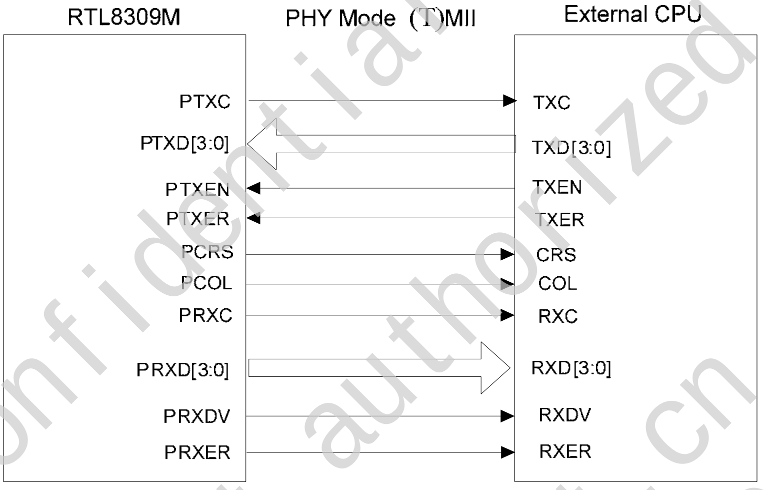

Figure 10. PHY Mode (T)MII Signal Diagram

7.3.5.2 MAC Mode (T)MII

MAC mode (T)MII means (T)MII at the External CPU drives the transmitting and receiving reference clock. Figure 11 shows the signal diagram for MAC mode (T)MII. MTXER/MRXER/MCOL/MCRS are not connected in TMII MAC mode.

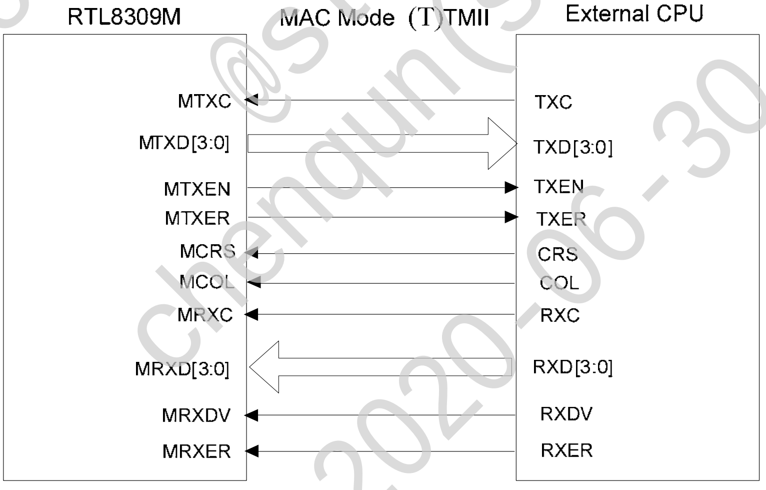

Figure 11. MAC Mode (T)MII Signal Diagram

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7.3.5.3 RMII

RMII (Reduced MII) is used in 10/100Mbps mode only. The reference clock pin of the RTL8309M's RMII can be configured to output a 50MHz clock, or be driven by an external clock source. Figure 12 shows the signal diagram.

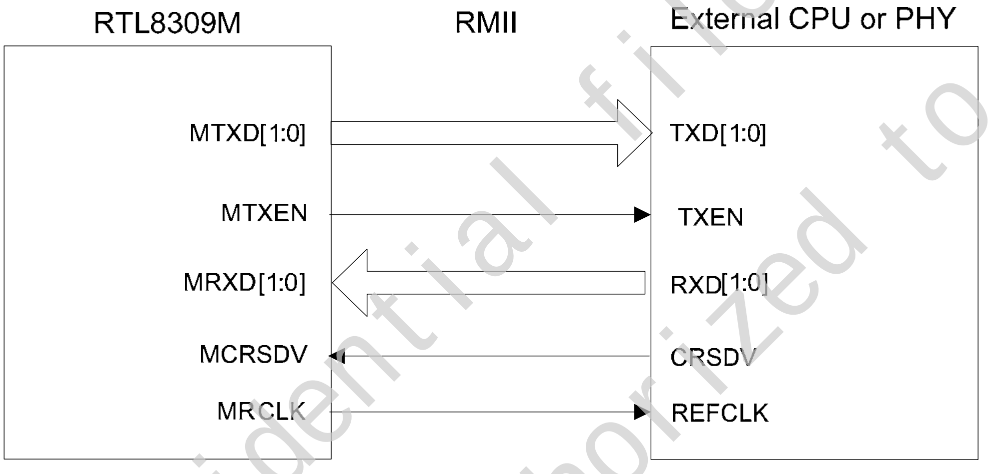

Figure 12. RMII Signal Diagram

7.3.6. Head-Of-Line Blocking

The RTL8309M incorporates a mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8309M first checks the destination address of the incoming packet. If the destination port is congested, the RTL8309M will discard this packet to avoid blocking the next packet, which is going to a non-congested port.

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7.3.7. Filtering/Forwarding Reserved Control Frame

The RTL8309M supports the ability to forward or drop the frames of the IEEE 802.1 specified reserved Ethernet multicast addresses.

Table 11. Reserved Ethernet Multicast Addresses

B: Broadcast (Search the Look-Up Table) D: Drop

Assignment	Value	Available Action
Bridge Group Address	01-80-C2-00-00-00	D, B (Default)
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01	D (Default), B
IEEE 802.3ad Slow_Protocols-Multicast Address	01-80-C2-00-00-02	D (Default), B
IEEE 802.1X PAE Address	01-80-C2-00-00-03	D, B (Default)
Reserved for Future Standards	01-80-C2-00-00-04~01-80-C2-00-00-0D, 01-80-C2-00-00-0F	D (Default), B
LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address	01-80-C2-00-00-0E	D, B (Default)
All LANs Bridge Management Group Address	01-80-C2-00-00-10	D (Default), B
Reserved for 01-80-C2-00-00-1x	01-80-C2-00-00-11~01-80-C2-00-00-1F	D, B (Default)
GMRP Address	01-80-C2-00-00-20	D (Default), B
GVRP Address	01-80-C2-00-00-21	D, B (Default)
Reserved for use by Multiple Registration Protocol (MRP) Applications	01-80-C2-00-00-22~01-80-C2-00-00-2F	D (Default), B
802.1ag PDU CCM/LTM	01-80-C2-00-00-31~ 01-80-C2-00-00-3F	D, B (Default)

7.3.8. Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table non-convergence. Frames are transmitted from Switch1 to Switch 2 via Link 1, and then returned to Switch 1 via Link 2.

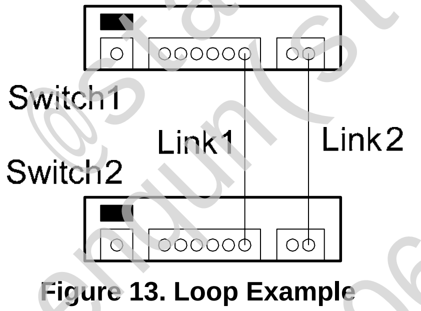

Figure 13. Loop Example

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The loop detect function can be enabled/disabled via strapping pin or registers. When the loop detection function is enabled, the RTL8309M sends out a broadcast 64-byte loop frame (the frequency is configured by register) and sniffs for the sent loop frame on each port to detect whether there is a network loop (or bridge loop). If a loop is detected, the RTL8309M will drive the external LEDs and buzzer alarm.

- The LED driven by the LDIND pin will blink
- The LEDs driven by port LED pins (see Table 5, page 11) of the ports on which the network loop is detected will all blink simultaneously
- The buzzer driven by the LDIND pin will buzz at the same frequency as the LED blinks

Both passive and active buzzers can be supported. The resonant frequency for the passive buzzer is approximately 2kHz. The buzzer and all LEDs will turn on/off simultaneously. In Figure 14, T1 is the turned-off period and T2 is the turned-on period. T1 and T2 are equal and can be configured to 400ms or 800ms.

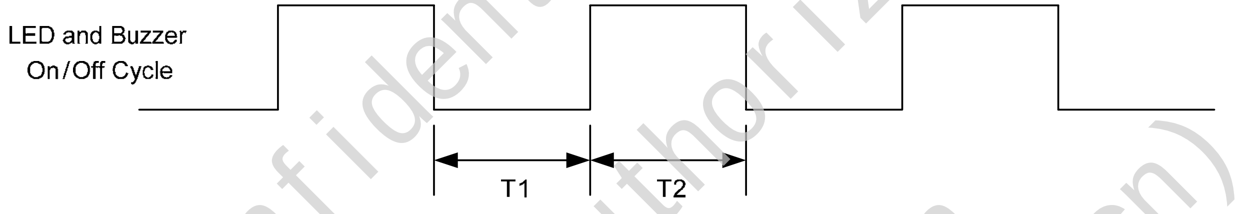

Figure 14. LED and Buzzer Control Signal for Loop Detection

Loop status, LED, and buzzer indications can be cleared when one of the following conditions occurs.

- Loop frame is not detected in the next loop detection period
- The loop port links down

The Loop frame length is 64 bytes. Its format is shown below.

Table 12. Loop Frame Format

48-bit	48-bit	16-bit	16-bit	12-bit	4-bit	352-bit	16-bit
FFFF FFFF FFFF	SID	8899	2300	000	TTL	0000	CRC

In order to achieve loop detection, each switch device needs a unique SID (the source MAC address). If an EEPROM is not used, a unique SID should be assigned via SMI after reset. The TTL (Time-To-Live) field is used to avoid a storm triggered by the loop frame. The TTL field in the loop frame will decrease by 1 when it passes through an RTL8309M whose MAC address is not equal to the SID of the loop frame. The RTL8309M will drop a loop frame in which the TTL is the minimum value (0001 is the minimum value. 0000, meaning 16, is the maximum value). The initial value of the TTL field can be configured via SMI or EEPROM.

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In Figure 15, device A, B, and C are in a loop. Device D connects to device B. Device D generates a loop frame with an initial TTL value 3 then sends to device B. When the loop frame arrives at device C, the TTL value decreases to 2. It turns to 1 when the loop frame is transmitted to device A, and then the loop frame is dropped by the device A. If device D generates loop frames without the TTL mechanism, the loop frames will cause a storm in the loop of devices A, B, and C. The RTL8309M provides an option to assign high priority to loop frames to reduce the possibility of erroneous loop frame dropping, and thereby enhance loop detection.

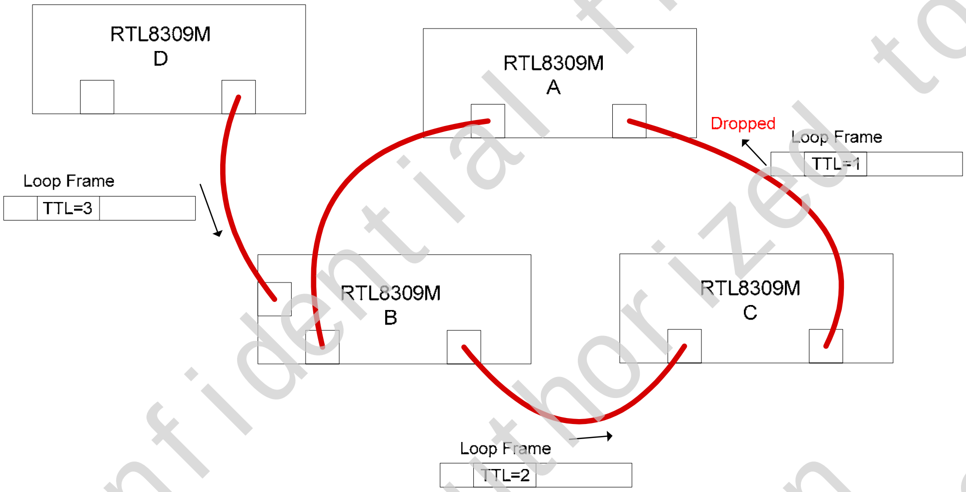

Figure 15. Loop Example 2

7.3.9. Reg.0.14 PHY Digital Loopback Return to Internal

The digital loopback mode of the PHY (return to internal MAC) may be enabled on a per-port basis by setting MII Reg.0.14 to 1. In digital loopback mode, the TXD of the PHY is transferred directly to the RXD of the PHY, with TXEN changed to CRS_DV, and returns to the MAC via an internal MII. The data stream coming from the MAC will not egress to the physical medium, and an incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps full duplex or 100Mbps full duplex mode. This function is especially useful for diagnostic purposes. For example, a NIC can be used to send broadcast frames into Port 0 of the RTL8309M and set Port 1 to Reg0.14 Loopback. The frame will be looped back to Port 0, so the received packet count can be checked to verify that the switch device is good. In this example, Port 0 can be 10M or 100M, and full or half duplex.

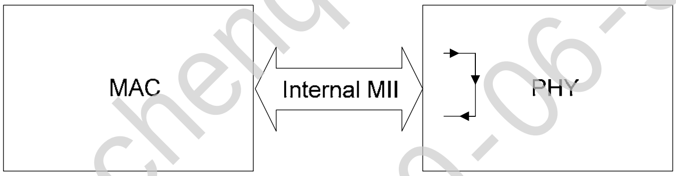

Figure 16. Reg. 0.14 Loopback

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As the RTL8309M only supports digital loopback in full duplex mode, PHY Reg.0.8 for each port will always be kept on 1 when digital loopback is enabled. The digital loopback only functions on broadcast packets (DA=FF-FF-FF-FF-FF-FF). In loopback mode, the link LED of the loopback port should always be ON, and the Speed and Duplex LED combined to reflect the link status (100full/10full) correctly, regardless of what the previous status of this loopback port was.

7.3.10. LDO for 1.0V Power Generation

The RTL8309M can use an internal LDO to generate 1.0V from a 3.3V power supply. This 1.0V is used for the digital core and analog receiver circuits. Do not use the LDO for other chips, even if the rating is enough.

Do not connect an inductor (bead) directly between the V10OUT pin and AVDDLPLL pin. This will adversely affect the stability of the 1.0V power to a significant degree. Please refer to the reference design for details.

7.3.11. Crystal/Oscillator

When using a crystal, the RTL8309M should connect a loading capacitor from each pin of XI and XO to ground. Whether using an oscillator or driving an external 25MHz clock from another device, the external clock should be fed into the XI pin. The following table shows the requirements of the crystal and oscillator.

Table 13. Crystal and Oscillator Requirements

Nominal Frequency	25.000 MHz
Frequency Tolerance	±50ppm Max.
Temperature Characteristics	±50ppm in Operating Temperature Range
Equivalent Series Resistance of Crystal	50 Ohm Max.
XTALI/OSC Input Clock Jitter Tolerance (in 5KHz to 2.5MHz Range)	250ps Max.
Duty Cycle	40%~60%

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8. Advanced Function Description

8.1. ACL Function

The ACL (Access Control List) holds 16 entries. When a packet is received, its source port, destination port (if a TCP or UDP packet) or EtherType code (if a non-IP packet), are recorded and compared to current ACL entries. If they are matched, and if physical port and protocol are also matched, the entry is valid.

In an ACL entry, the physical port bit value of 0b0000 to 0b1000 represents ports 0 to 8 of the RTL8309M; the value 0b1001 indicates that the entry is invalid; and the value 0b1010 means that the entry can be valid whichever port the packet comes from.

For the protocol bit:

- 0b00 indicates an EtherType valid entry
- 0b01 indicates a TCP valid entry
- 0b10 indicates a UDP valid entry
- 0b11 indicates a TCP or UDP valid entry

If a received packet matches multiple entries, the entry with the lower address is valid. If the entry is valid, the action bit and priority bit are applied.

- If the action bit is ‘Drop’, the packet will be dropped
- If the action bit is ‘CPU’, the packet will be trapped to the CPU instead of forwarded to a non-CPU port, except where it has been determined by other rules (other than ACL rules), that it should be dropped
- If the action bit is ‘Permit’, ACL rules will have no effect
- If the action bit is ‘Mirror’, the packet will be forwarded to the mirror port after it is sent to its destination port (the mirror port is the destination port in the port mirror mechanism)

The priority bit will take effect if the action bits are CPU, Permit, or Mirror, and is used to determine the packet queue ID according to the priority assignment mechanism.

8.2. MAC Limit

The RTL8309M supports the capability of limiting the number of MAC addresses that are learned. The learned MAC addresses of each port, and the total learned MAC addresses of any combination of multi ports can be limited. The limit thresholds of each port can be configured independently from 0 to 31; 0 to 255 for multi ports.

There is a counter for each of the limits. The counter will be decremented if a counted MAC address ages out. Deleting or creating entries in the LUT via register setting will not affect these counters. When the MAC limit of port(s) reached, the received packet on the corresponding port, which is not learned or is learned but is not the current ingress port, will be dropped and not be learned.

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8.3. Port Isolation

The port isolation function allows the RTL8309M to restrict traffic flow flexibly. The traffic between two physical ports can be isolated independently and simultaneously. When port isolation is enabled, received traffic from these two ports can never be forwarded to the other.

8.4. VLAN Function

8.4.1. VLAN Description

The RTL8309M supports 16 VLAN groups with the 16-entry VLAN table (see Table 14 and Table 15). These can be configured as port-based VLANs and/or IEEE 802.1Q tag-based VLANs. The RTL8309M supports four IVLs, with the mapping information in the VLAN table. The contents of the VLAN table can be configured via SMI or EEPROM. Multiple ingress filtering and egress filtering options provide various VLAN admit rules for the RTL8309M. The RTL8309M also provides flexible VLAN tag insert/remove function based on port and VID.

Table 14. VLAN Table

Entry Index	VLAN ID	Membership	UNTAG_MSK	FID
VLAN Entry 0	VLAN ID A[11:0]	VLAN ID A membership [8:0]	VLAN ID A UNTAG_MSK [8:0]	FID[1:0]
VLAN Entry 1	VLAN ID B [11:0]	VLAN ID B membership [8:0]	VLAN ID B UNTAG_MSK [8:0]	FID[1:0]
……	……	……	……	……
VLAN Entry 15	VLAN ID P [11:0]	VLAN ID P membership [8:0]	VLAN ID P UNTAG_MSK [8:0]	FID[1:0]

Table 15. VLAN Entry

Field	Description	Bits
VID	The VLAN ID for Search. The VID of the ingress packet will be compared with this field.	12
MBR	VLAN Member Port Set. If the bit in this field is '1', the corresponding port is a member port of the VLAN specified by the VID field.	6
UNTAG SET	VLAN Untag Set. If the bit in this field is '1', egress packets from the corresponding port will be VLAN-untagged.	6
PRIORITY	VID-Based Priority. The priority assigned to all ingress packets of the VLAN specified by the VID field.	2
FID	The FID is Used by Lookup Table for IVL Application.	12

The main VLAN features of the RTL8309M are as follows:

- Supports up to 16 VLAN groups
- Flexible IEEE 802.1Q port/tag-based VLAN
- Four IVLs
- Leaky VLAN for ARP broadcast/unicast/multicast packets

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- Leaky inter-VLAN mirror function
- VLAN tag Insert/Remove function

8.4.2. Port-Based VLAN

The 16 VLAN membership registers designed into the RTL8309M provide full flexibility for users to configure the member ports to associate with different VLAN groups in the VLAN table. Each port can join more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members. The RTL8309M supports VLAN indexes for each port to individually index this port to one of the 16 VLAN membership registers. A port that is not included in a VLAN's member set cannot transmit packets to this VLAN.

For non-VLAN tagged frames, the RTL8309M performs port-based VLAN. The VLAN ID associated with the port-based VLAN index setting is the Port VID (PVID) of this port. The VLAN tag with the ingress port's PVID can be inserted (or replace the VID with a PVID for VLAN-tagged packets) into the packet on egress. The RTL8309M also provides an option to admit VLAN tagged packets with a specific PVID only. When IEEE 802.1Q tag-aware VLAN is enabled, the VLAN tag admit control and non-PVID discard are enabled at the same time. Non-tagged packets and packets with an incorrect PVID will be dropped.

The RTL8309M supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. The PVID in the inserted (or replaced) VLAN tag on egress can indicate the source port of the packet. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8309M also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

8.4.3. IEEE 802.1Q Tagged-VID Based VLAN

The RTL8309M supports 16 VLAN entries to perform IEEE 802.1Q-tagged VID-based VLAN mapping. The RTL8309M uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. If the VID of a VLAN-tagged frame does not match any of the 16 VLAN entries, the RTL8309M will drop the frame. Otherwise, the RTL8309M compares the explicit identifier in the VLAN tag with the 16 VLAN IDs to determine the VLAN association of this packet, and then forwards this packet to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8309M performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8309M performs only port-based VLAN mapping both on non-tagged and tagged frames.

8.4.4. Insert/Remove/Replace Tag

The RTL8309M supports the VLAN Insertion/Removal/replacing action for each port. The 802.1Q VLAN tags can be inserted, removed, or replaced based on the port's setting.

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8.4.5. Ingress and Egress Rules

The RTL8309M provides flexible VLAN ingress and egress rules to permit comprehensive traffic control. The RTL8309M can filter packets on ingress according to the tag condition of the packet. For a normalized VLAN application and VLAN translation application, each of the RTL8309M ports can be independently configured to:

- 'admit all frames'
- 'admit only tagged frames'
- 'admit only untagged frames'

Note: The priority tagged frame (VID=0) will be treated as an untagged frame.

The RTL8309M also can optionally discard a frame associated with a VLAN of which the ingress port is not in the member set.

For the egress filter, the RTL8309M drops the frame if this frame belongs to a VLAN but its egress port is not one of the VLAN's member ports. However, there are 5 leaky options to provide exceptions for special applications.

- 'Unicast leaky VLAN' enables inter-VLAN unicast packet forwarding. That is, if the layer 2 lookup table search has a hit, then the unicast packet will be forwarded to the egress port, ignoring the egress rule
- 'Multicast leaky VLAN' enables inter-VLAN multicast packet forwarding. Packets may be flooded to all the multicast address group member sets, ignoring the VLAN member set domain limitation
- 'Broadcast leaky VLAN' enables inter-VLAN broadcast packet forwarding. Packets may be flooded to all the other ports, ignoring the VLAN member set domain limitation
- 'ARP leaky VLAN' enables broadcasting of ARP packets to all other ports, ignoring the egress rule
- 'Inter-VLAN mirror function' enables the inter-VLAN mirror function, ignoring the VLAN member set domain limitation. The default value is 'Enable the inter-VLAN mirror'

8.5. IEEE 802.1p Remarking Function

The RTL8309M provides IEEE 802.1p Remarking ability. Each port can enable or disable IEEE 802.1p Remarking ability.

In addition, there is a RTL8309M global IEEE 802.1p Remarking Table. When one port enables 802.1p Remarking ability, 2-bit priority (not QID) determined by the RTL8309M is mapped to 3-bit priority according to the 1p Remarking Table.

If the port's 1p remarking function is enabled, transmitting VLAN tagged packets will have the 1Q VLAN tag's Priority field replaced with the 3-bit 1p remarking Priority.

When the VLAN tags are inserted to non-tagged packets, the inserted tag's priority will accord with the 1p remarking table, even if the port's 1p remarking function is disabled. When the VLAN tag is replaced on tagged packets and the 1p remarking function is disabled, the VLAN tag's VID will be replaced but the priority will not change. For a VLAN-tagged packet, the VID and 3-bit priority can be replaced by the RTL8309M independently.

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8.6. QoS Function

8.6.1. Bandwidth Control

8.6.1.1 Output (TX) Bandwidth Control

The RTL8309M supports MIN-MAX packet scheduling.

Packet scheduling offers three modes:

- Type I leaky bucket, which specifies the average rate of one queue (see Figure 17; only Q2 and Q3 have leaky bucket, Q0 and Q1 do not). The queue rate can be configured from 0kbps to the line rate in steps of 64kbps
- Weighted Round Robin (WRR), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue
- Port bandwidth control (type II leaky bucket) to control the bandwidth of the whole port. The port rate can be configured from 0kbps to the line rate in steps of 64kbps

In addition, the RTL8309M can select one of the two sets of packet-scheduling configurations according to the packet-scheduling mode. Figure 17 shows the RTL8309M packet-scheduling diagram.

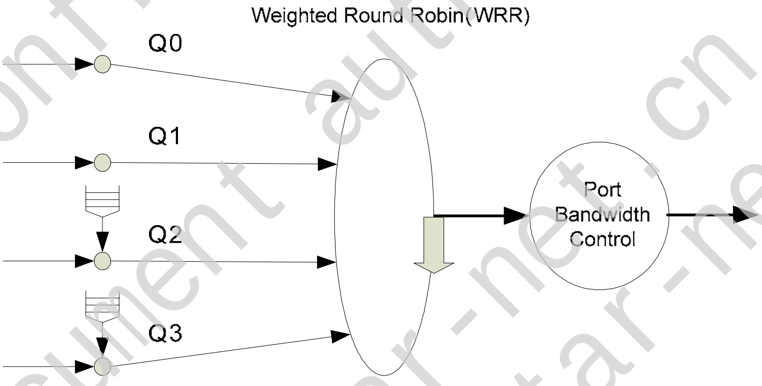

Figure 17. Packet-Scheduling Diagram

Weighted Round Robin (WRR)

WRR adds weighting on the basis of Round Robin; for example, assume Q3:Q2:Q1:Q0: 4:3:2:1, then the transmit order will be:

Q0->
Q1->Q1->
Q2->Q2->Q2->
Q3->Q3->Q3->Q3->

WRR guarantees a minimal packet rate for one queue only.

If there is strict priority (only in Q2 and Q3) and WRR at the same time, the queue with strict priority has higher priority than WRR. When the scheduler scans queues, queues with strict priority are scanned first, and then the other queues are scanned according to WRR. If there is more than one queue with strict priority, the queue with the bigger QID has higher priority.

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8.6.1.2 *Input (RX) Bandwidth Control*

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on flow control status. The input bandwidth can also be configured from 0kbps to the line rate in steps of 64kbps.

8.6.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8309M can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8309M identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- IEEE 802.1p/Q VLAN Priority Tag
- DSCP Priority field
- IP Address
- Reassigned priority
- RLDP priority

Below is a block diagram of the priority assignment.

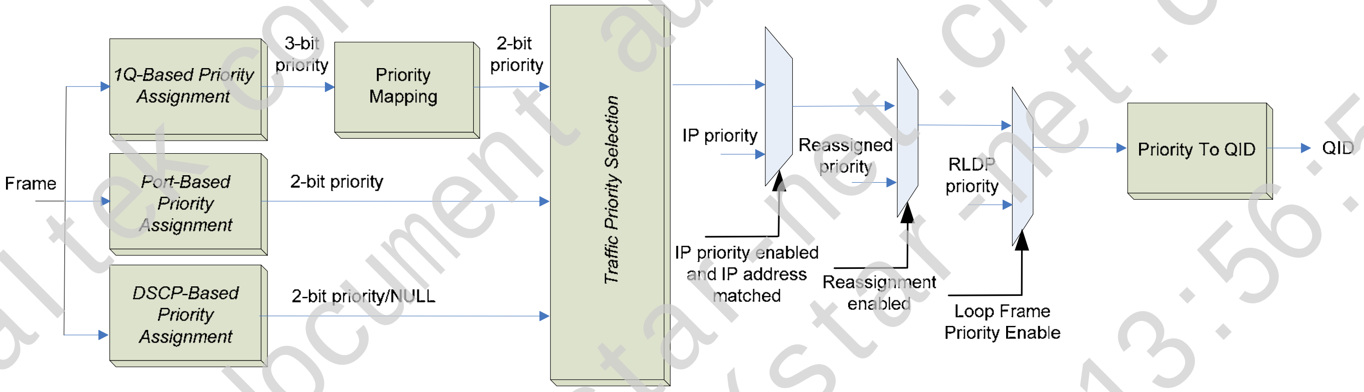

Figure 18. RTL8309M Priority Assignment Diagram

8.6.2.1 *Queue Number Selection*

In the RTL8309M, the output queue number can be set. All ports follow a global configuration. The maximum number of output queues per port is 4. After changing the queue number via SMI (Serial Management Interface), the external device must perform a soft reset in order to update the configuration.

8.6.2.2 *Port-Based Priority Assignment*

Each physical port is assigned a 2-bit priority level. Packets received from a high-priority port are sent to the high-priority queue of the destination port. Port-based priority can be disabled by register setting.

8.6.2.3 IEEE 802.1p/Q-Based Priority Assignment

In IEEE 802.1Q-based priority assignment, when a packet is VLAN-tagged or priority-tagged, the 3-bit priority is specified by tag. When a packet is untagged, the 802.1Q-based priority is assigned to the default 2-bit priority information of a physical port. So, each port must provide a default 2-bit priority (every received packet must be assigned a 2-bit 1Q-Based Priority). When the priority comes from a packet, the 1Q-based priority is acquired by mapping 3-bit tag priority to 2-bit priority though an RTL8309M 1Q-based Priority Mapping Table. The 1Q-based priority can be disabled.

8.6.2.4 DSCP-Based Priority Assignment

DSCP (Differentiated Services Code Point)-based priority assignment maps the DSCP of an IP packet to 2-bit priority information through a DSCP to priority table, as DSCP is only in the IP packet. A non-IP packet (such as a Layer 2 frame, ARP, etc) will get a NULL instead of a 2-bit priority. For an IPv6 IP header, DSCP-based priority assignment acquires the DSCP value according to the class of IPv6 header.

In the RTL8309M, DSCP-based priority assignment provides a DSCP to Priority Table of all DSCP value. If the DSCP of a packet is not matched in the table, the DSCP-based priority is 2'b00, The DSCP-based priority can be disabled by register.

8.6.2.5 IP Address-Based Priority

When IP-based priority is enabled, any incoming packets with source or destination IP address equal to the configuration in register IP Priority Address [A] and IP Priority Mask [A], or IP Priority Address [B] and IP Priority Mask [B] will be set to a 2-bit priority.

IP priority [A] and IP priority [B] may be enabled or disabled independently. IP address-based priority can be enabled or disabled by the control register.

8.6.2.6 Reassigned Priority

RL8309M can reassign the priority mainly according to the packets' DMAC information. This function is used to differentiate the priority of the Layer 2 control packet, broadcast packet, multicast packet, unicast packet, and so on.

8.6.2.7 RLDP-Based Priority

To support the loop detection effectively, the RTL8309M provides the RLDP-based priority assignment. When it is enabled, the pre-defined priority will be assigned to all RLDP packets.

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8.6.2.8 Packet Priority Selection

As one received packet may simultaneously support several priority assignment mechanisms, e.g., Port-Based Priority, 1Q-Based Priority, DSCP-Based Priority, it may get several different priority values.

- RLDP-based priority has the highest priority
- If RLDP-based priority is disabled, the final priority is equal to the reassigned priority
- If RLDP-based priority and reassigned priority is disabled, the final priority is equal to the IP address priority
- If RLDP-based priority, reassigned priority and IP address priority are disabled, the following rules are used to decide a final priority for the other five types of priority

There is a 2-bit register for each of the three types of priority that represent the weight of the priority. The higher value in the register indicates a higher weight for the priority. If more than one of the three types of priority is the same, the final priority will be the one of the three types, whose priority value is greatest.

Queue Priority Mapping

The 2-bit priority has four numbers; however, every port has at most four output queues, so every port needs a User Priority to Traffic Class Mapping Table to map the priority to QID. A set of Traffic Class Mapping Tables is provided for each port independently. There is a mechanism to prevent a problem caused by mapping the traffic to an unused queue. For example, when a port's queue number is 2, the queue 2 and queue 3 are not used and mapping the traffic to queue 2 or queue 3 will cause the system to crash. In the mechanism, traffic mapped to the unused queue will be forced to the highest used queue (queue 2 in a 3-queue case, queue 1 in a 2-queue case, queue 0 in a 1-queue case). In the example, the traffic mapped to a port's queue 2 or queue 3 will be forwarded to queue 1.

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8.7. *Lookup Table Function*

8.7.1. Function Description

- 2048-entry lookup table (LUT)
- 4-way entry for each entry index
- Supports LRU (Least Recently Used) function for lookup table learning

8.7.2. Address Search, Learning, and Aging

Received packets are forwarded according to the information learned or written into the LUT. When a packet is received, the RTL8309M tries to retrieve learned information and assign a forwarding destination port to the packet.

The 48-bit destination MAC address (DA) of the received packet and the 2-bit FID are used to calculate a 9-bit index value. The hash algorithm uses all 48 bits of the MAC address and 2 bits of the FID. The hash algorithm is shown below.

Index 0 = MAC4 ^ MAC11 ^ MAC18 ^ MAC25 ^ MAC32

Index1 = MAC3 ^ MAC10 ^ MAC17 ^ MAC24 ^ MAC47

Index2 = MAC2 ^ MAC9 ^ MAC16 ^ MAC39 ^ MAC46

Index3 = MAC1 ^ MAC8 ^ MAC31 ^ MAC38 ^ MAC45

Index4 = FID1 ^ MAC0 ^ MAC23 ^ MAC30 ^ MAC37 ^ MAC44

Index5 = FID0 ^ MAC15 ^ MAC22 ^ MAC29 ^ MAC36 ^ MAC43

Index6 = MAC7 ^ MAC14 ^ MAC21 ^ MAC28 ^ MAC35 ^ MAC42

Index7 = MAC6 ^ MAC13 ^ MAC20 ^ MAC27 ^ MAC34 ^ MAC41

Index8 = MAC5 ^ MAC12 ^ MAC19 ^ MAC26 ^ MAC33 ^ MAC40

As the 9-bit MAC addresses, MAC[13:15] and MAC[0:5], are not stored in the LUT entries, these MAC address bits should be calculated from the index information via the following method when the hash algorithm is selected.

MAC0 = Index4 ^ FID1 ^ MAC23 ^ MAC30 ^ MAC37 ^ MAC44

MAC1 = Index3 ^ MAC8 ^ MAC31 ^ MAC38 ^ MAC45

MAC2 = Index2 ^ MAC9 ^ MAC16 ^ MAC39 ^ MAC46

MAC3 = Index1 ^ MAC10 ^ MAC17 ^ MAC24 ^ MAC47

MAC4 = Index0 ^ MAC11 ^ MAC18 ^ MAC25 ^ MAC32

MAC5 = Index8 ^ MAC12 ^ MAC19 ^ MAC26 ^ MAC33 ^ MAC40

MAC13 = Index7 ^ MAC6 ^ MAC20 ^ MAC27 ^ MAC34 ^ MAC41

MAC14 = Index6 ^ MAC7 ^ MAC21 ^ MAC28 ^ MAC35 ^ MAC42

MAC15 = Index5 ^ FID0 ^ MAC22 ^ MAC29 ^ MAC36 ^ MAC43

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The hashed index key is used to locate a matching LUT entry. There are 4 entries sharing one index key (Table 16). This is called a 4-way hash. It is helpful to minimize address collisions in the address learning process. The address search engine compares the DA packet with the data in 4 entries, from entry 3 to entry 0. The final forwarding destination is abstracted from the first matching entry. If the address search fails to return a matching LUT entry, the packet will be flooded to appropriate ports.

Table 16. L2 Table 4-Way Hash Index Method

Index	Entry 0	Entry 1	Entry 2	Entry 3
0x00	MAC Addr 0	MAC Addr 1	MAC Addr 2	MAC Addr 3
0x01	MAC Addr 4	MAC Addr 5	MAC Addr 6	MAC Addr 7
0x02	MAC Addr 8	MAC Addr 9	MAC Addr 10	MAC Addr 11
…	…	…	…	…
0x1FE	MAC Addr 2040	MAC Addr 2041	MAC Addr 2042	MAC Addr 2043
0x1FF	MAC Addr 2044	MAC Addr 2045	MAC Addr2046	MAC Addr 2047

Address learning is the gathering process and storing of information from received packets for the future purpose of forwarding frames addressed to the receiving port. The information includes the source MAC address (SA) and the receiving port. As with the hash algorithm, an address search is used in address learning. The SA of the received packet is used to calculate the entry index. The receiving port information and the aging timer of the first matching entry will be updated when an address is learned. If there is no matching entry, the packet's information will be 'learned' into the first empty entry. The SA will not be learned when all of the 4 entries are occupied. The address learning process can be disabled on a per-port basis via register setting.

For unicast packet learning & search, and multicast packet search, the RTL8309M applies the same 4-way hash algorithm.

Address aging is used to keep the contents of the learned address table updated in a dynamic network topology. The look-up engine will update the aging timer of an entry whenever the corresponding SA appears. An entry will be invalid (aged out) if its aging timer is not refreshed by the address learning process during the aging time period. The aging time of the RTL8309M is between 200 and 400 seconds. The RTL8309M also supports a fast aging function that is used to age all dynamic entries within 1ms.

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8.7.3. Lookup Table Definition

In traditional switch learning, if a MAC address hash collision occurs then the later MAC address in the collision will not be learned into the lookup table. The LRU function attempts to resolve this problem.

When Enable LRU = 0b1, then the LRU function is enabled. If the Source MAC address of the incoming packet encounters a hash collision during the learning process and when the 4-way entries are all occupied, then the switch will learn the address in one of the 4-way entries using the LRU aging timer. The criteria for selecting the entry to over-write is comparing via the aging timer and choosing the oldest entry. If the aging timer of the 4 entries are the same, then the entry with the highest Entry_Address[1:0] value is selected to be over-written.

8.8. MIBS Function

8.8.1. MIB Counter Description

The RTL8309M implements twelve 32-bit and two 64-bit MIB Counters on each port for traffic management and diagnostic purposes. The fourteen MIB counters are TX Byte Counter, RX Byte Counter, TX Packet Counter, RX Packet Counter, RX Drop Counter, RX CRC Counter, RX Fragment Counter, TX Broadcast Packet Counter, RX Broadcast Packet Counter, TX Multicast Packet Counter, RX Multicast Packet Counter, TX Unicast Packet Counter, RX Unicast Packet Counter, RX Symbol Error Counter.

The TX Byte Counter and RX Byte Counter are 64-bit MIB Counters, which include two 32-bit counters. There is also an on-off register for each port to enable or disable/clear MIB Counters. Pause frame on/off is not counted in any condition. These MIB Counters are described below:

- TX Byte Counter:
  TX byte count. For half duplex collisions cause TX fragment packets, these bytes are not included in this counter. This counter is incremented once for every data byte of a transmitted packet.
- RX Byte Counter:
  RX byte count. This counter is incremented once for every data byte of a received and forwarded good packet. RX byte count includes both forwarded and dropped good packets. For mirror RX forwarded packets, if these are not good packets they will not be counted
- TX Packet Counter:
  TX packet count. For half duplex collisions cause TX fragment packets, these packets are not included in this counter. This counter is incremented once for every packet of a transmitted packet.
- RX Packet Counter:
  RX packet count. This counter is incremented once for every packet of a received and forwarded good packet. RX packet count includes both forwarded and dropped good packets. For mirror RX forwarded packets, if these are not good packets they will not be counted
- RX Drop Counter:
  RX drop packet count. Packet drop events could be due to lack of resources, local packet, etc. If the mirror RX function is enabled and the packets are only received by the mirror port, these packets are also included in the mirrored port's dropped packet counter. Packet lengths less than 64 bytes are not included

- RX CRC Counter:
  RX CRC error packet count. This counter is incremented once for every received packet with a length more than 64 bytes but with a CRC error. Oversize packets are also included in this counter
- RX Fragment Counter:
  RX fragment, collision, and undersize packet count. These packet lengths are less than 64 bytes
- TX Broadcast Packet Counter:
  TX broadcast packet count. This counter is incremented once for every broadcast packet of a transmitted packet.
- RX Broadcast Packet Counter:
  RX broadcast packet count. This counter is incremented once for every broadcast packet of a received and forwarded good Broadcast packet.
- TX Multicast Packet Counter:
  TX multicast packet count. This counter is incremented once for every Multicast packet of a transmitted packet.
- RX Multicast Packet Counter:
  RX multicast packet count. This counter is incremented once for every multicast packet of a received and forwarded good multicast packet.
- TX Unicast Packet Counter:
  TX unicast packet count. This counter is incremented once for every unicast packet of a transmitted packet.
- RX Unicast Packet Counter:
  RX unicast packet count. This counter is incremented once for every unicast packet of a received and forwarded good packet.
- RX Symbol Error Counter:
  RX symbol error count. This counter is incremented once for every symbol error packet of a received and forwarded good packet.

As data can only be read 16-bits at one time, when reading these 32-bit counters through an SMI interface, they should always read low bits (bit [15:0]) first. Both the low 16 bits and high 16 bits are latched, and it should read the high bits register in the immediately following a read cycle.

8.8.2. MIB Counter Enable/Clear

After power on reset, the counters are all reset to 0. A read access of the MIB counter will not reset the counter to 0. When power-on occurs, the counters will be cleared to 0.

An Enable/Disable MIB Counter register is provided for all ports. When 'EnMIBCounter' is asserted to 1, all port MIB counterwill be enabled. If 'EnMIBCounter' is asserted to 0, all port MIB counters will be disabled. When 'EnMIBCounter' is asserted to 1, then set per port 'PnCounterStart' to 1, the corresponding port starts counting. If set 'PnCounterStart' to 0, the corresponding port stops counting. A Reset MIB Counter register is provided per port, when 'PnCounterReset' is asserted to 1, the corresponding port counter is cleared to 0, at the same time, 'PnCounterReset' is auto returned to 0.

8.9. Storm Filter Function

The RTL8309M can effectively control four-types of broadcast storms; those caused by broadcast packets, multicast packets, unknown multicast packets, and unknown DA unicast packets.

Note: Broadcast packets discussed here are packets whose DA is ff-ff-ff-ff-ff-ff.

Multicast packets include all multicast packets and only unknown multicast packets, which are those whose DA is a multicast address, but excluding 01-80-C2-00-00-xx.

An unknown DA unicast packet is a packet whose DA is a unicast address and is not found in the lookup table of the switch.

The RTL8309M can configure a storm filter rate for these four packet types, and the rate unit can be configured as packet-based or byte-based via registers. The storm filter rate limits the packet forwarding rate to less than the rate threshold.

8.10. IGMP & MLD Snooping Function

The RTL8309M supports IGMP v1/v2/v3 and MLD v1/v2 snooping. The RTL8309M can trap all IGMP and MLD packets to the CPU port. The CPU processes these packets, gets the IP multicast group information of all ports, and writes the correct multicast entry to the lookup table via SMI. The RTL8309M provides an option to drop or broadcast multicast packets when the multicast MAC address does not exist in the lookup table.

IGMP & MLD snooping only operates when the CPU port function is enabled. If the CPU port function and IGMP snooping are both enabled, the RTL8309M traps all packets to the CPU where:

- EtherType is 0x0800 and the protocol field in the IP header is 0x02 (for PPPoE packets the EtherType is 0x8864 and PPP protocol=0x0021)

If the CPU port function and MLD snooping are both enabled, the RTL8309Mwill trap all packets to the CPU where:

- EtherType is 0x86DD and the next header field in the IPv6 header is 0x00 (for PPPoE packets EtherType is 0x8864 and PPP protocol=0x0057) to CPU

MLD packets have three characteristics:

1. EtherType=0x86DD (2bytes) (for PPPoE packets, EtherType = 0x8864 and PPP protocol = 0x0057)

2. 'Next header' = 0 (1byte) in IPv6 header

3. 'Route alert option' = 0x05020000 (4bytes) in hop-by-hop option header

If a packet matches the first two characteristics, it will be trapped to the CPU. The CPU will then check the 'Route alert option' and other fields to determine whether the packet is an MLD packet.

To avoid a loop condition, IGMP and MLD packets received from the CPU port will never be trapped, even if all options enable trapping action.

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8.11. CPU Tag Function

The RTL8309M can insert a CPU tag that contains source-port information to the packets sent to the CPU port.

There are four circumstances where the CPU tag is useful:

- The CPU needs the source-port information of the packets trapped to the CPU
- The CPU can use the CPU tag to inform the RTL8309M of the packet's destination port
- The CPU needs to assign specific priority to the packet, or get the final priority information of the packet trapped to the CPU
- The CPU needs to disable the learning ability of the RTL8309M when transmitting some specific traffic to the RTL8309M

The tag format is shown in Table 17.

Table 17. CPU Tag Format

15	8	7	0
EtherType(16-bit) [0x8899]			
Protocol (4-bit) [0x4]	Priority(2-bit)	DisLrn(1-bit)	Tx/Rx(9-bit)

The CPU tag is inserted behind the packet's SA. The EtherType field of the tag is assigned by register. Its default value is 0x8899, which is a Realtek proprietary number. The following protocol field can be configured by register CPU_TAG_PROC; default value is 0x4.

When the RTL8309M inserts a CPU tag to a packet forwarded to the CPU, the priority field will be filled with the packet final priority from the QoS rule.

When the RTL8309M receives a packet with a CPU tag inserted by the CPU, the priority field indicates the CPU-assigned priority for this packet.

When the RTL8309M receives a packet with the CPU tag and the Disable/Enable Learning bit set to '1', it will not perform a LUT learning process for this packet. Note that if the CPU tag was inserted to the packet by the RTL8309M, the Disable/Enable Learning bit will be irrelevant.

The TX/RX field is RX when the CPU tag is inserted by the RTL8309M, and it indicates the packet's source port. The TX/RX field is TX when the CPU tag is inserted by the CPU, and it indicates the packet's destination port. If the TX field is '0', packets can be optionally dropped or forwarded based on the LUT search result.

The bit for TX/RX field to port mapping is shown in Table 18. Writing '1' in the field means the corresponding port is the source port (for RX) or destination port (for TX) of the packet.

Table 18. Bit to Port Mapping in CPU Tag

TX/RX MSB								LSB
Port 8	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1	Port 0

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CPU tag insertion is independent of IGMP & MLD snooping. All packets sent to the CPU port (including any packets unicast or broadcast to the CPU port) can be inserted with a CPU tag when CPU tag insertion is enabled. The RTL8309M also supports inserting a CPU tag into the packet only when the packet is trapped to the CPU (i.e., not normally forwarded to the CPU) due to special setting.

When CPU tag removal is enabled, if the EtherType matches the CPU tag content register and the following 4 bits are 0x4, the RTL8309M will remove the 32 bits following the SA of the packet. The RTL8309M then retrieves the CPU assigned priority in the tag and forwards it with the destination port information in the CPU tag.

There is an option for the RTL8309M to check a CPU-tagged packet's CRC, which can greatly reduce the external CPU's loading. Another configuration option enables or disables CPU tagged-packet awareness.

A typical application of the RTL8309M CPU tag function is shown in Figure 19.

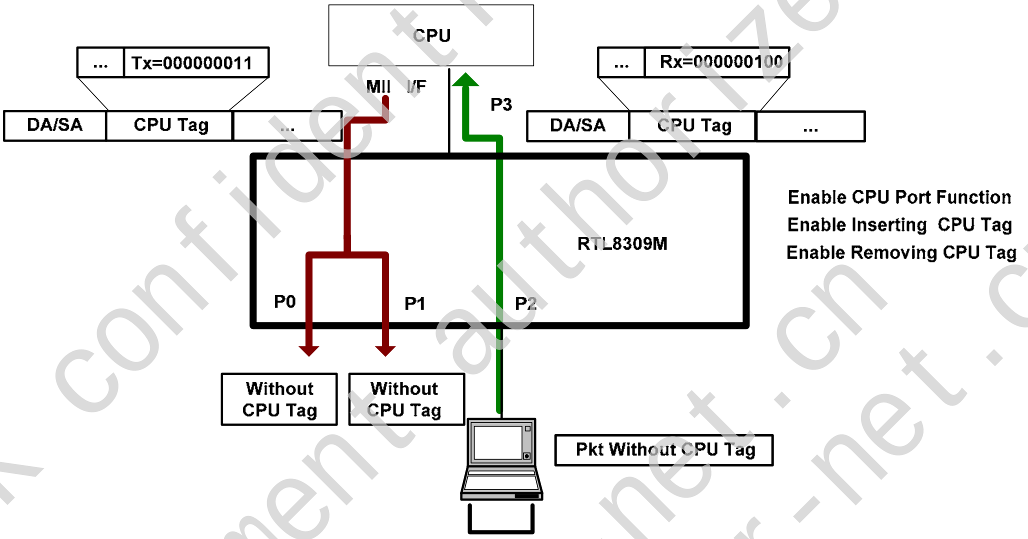

Figure 19. CPU Tag Application Example

8.12. IEEE 802.1x Function

The RTL8309M supports IEEE 802.1x Port-based/MAC-based Access Control.

When port-based access control and MAC-based access control are both enabled, only frames that comply with both port-based access control and MAC-based access control will be forwarded. The IEEE 802.1x Port-based/MAC-based Access Control rules will be ignored for the following two types of packets:

- CPU tagged packets (only when CPU tagged-packet awareness is disabled)
- Reserved control packets (which will be trapped to the CPU)

8.12.1. Port-Based Access Control

When a PC host connects to a RTL8309M-controlled switch, the switch will ask the PC host for authentication. The switch will transmit the information sent by the host to the authentication server for authenticating.

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- When the register 'Port-based Authorization status of 802.1x for Port x'=1, that is, the port is authenticated, its traffic will be normally received or sent
- When the register 'Port-based Authorization status of 802.1x for Port x'=0, that is, the port is not authenticated, its traffic will not be normally forwarded

The register 'Direction of 802.1x control for Port x' decides whether or not the traffic of other ports can be forwarded to the port.

- If 'Direction of 802.1x control for Port x'=0, packets need to pass 802.1x authorization in the input direction and the output direction for Port-Based Access Control
- If 'Direction of 802.1x control for Port x'=1, packets only need pass 802.1x authorization in the input direction for Port-Based Access Control. Output direction packets will bypass the 802.1x authorization rule

8.12.2. MAC-Based Access Control

MAC-based access control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the DTE using the MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

When the register bit 'Enable Mac-based authorization of 802.1x for Port x'=1, it means port n has MAC-based access control ability. In this condition, if a MAC address is authenticated by EAPOL, the 'Author' bit in the corresponding lookup table entry should be set to '1', which indicates that the address is authenticated. If a MAC address is unauthenticated, the 'Author' bit should be set to '0'. A received frame with unauthenticated source MAC address will be dropped or trapped to the CPU, which is determined based on the register 'Operation of 802.1x unauthorized frame'.

There is another register used for the control of MAC-based access:

- If the register 'Direction for 802.1x MAC-Based Access Control'=0, the forwarding packets need to pass 802.1x authorization in both the input direction and output direction for MAC-based access control.
- If 'Direction for 802.1x MAC-Based Access Control'=1, the forwarding packets only need pass 802.1x authorization in the input direction for MAC-based access control.

IEEE 802.1X MAC-based authentication processing is handled by the CPU and the authentication server. When a Source-MAC-Address is authorized, the CPU will write an 802.1X MAC-Based Entry (AUTH=1) into the MAC-Address-Table. The behavior is determined based on Table 19.

Table 19. IEEE 802.1x MAC-Based Entry

MAC-Based	Static	Auth	Description	Aging	Aging Out	Update MBR
0 (Disable)	0	0	General Dynamic Entry	Yes	Yes	Yes
0	0	1	802.1x Dynamic Entry (do not bind host to any specified port)	Yes	No	Yes
0	1	0	General Static Entry	Yes	No	No

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MAC-Based	Static	Auth	Description	Aging	Aging Out	Update MBR
0	1	1	802.1x Static Entry (bind host to a specified port)	Yes	No	No
1 (Enable)	0	0	General Dynamic Entry	Yes	Yes	Yes
1	0	1	802.1x Dynamic Entry (do not bind authenticated host to any specified port)	Yes	No	Yes
1	1	0	General Static Entry	Yes	No	No
1	1	1	802.1x Static Entry (bind authenticated host to a specified port)	Yes	No	No

8.13. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8309M supports four states for each port:

Disabled

The port will not transmit/receive packets, and will not perform learning.

Blocking

The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning.

Learning

The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets.

Forwarding

The port will transmit/receive all packets, and will perform learning.

The RTL8309M also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

Behaviors are shown in the following table.

Table 20. Behavior on TX_EN, RX_EN, and PSTAn

A: All packets
B: BPDU packet
D: Disable. RX will not learn; TX will not send any packets
L: Learn all packets, but do not forward

TX_EN	RX_EN	PSTAn	Description
0	0	00	RX (D) TX (D)
		01	RX (D) TX (D)
		10	RX (D) TX (D)
		11	RX (D) TX (D)

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A: All packets
B: BPDU packet
D: Disable. RX will not learn; TX will not send any packets
L: Learn all packets, but do not forward

TX_EN	RX_EN	PSTAn	Description
0	1	00	RX (D) TX (D)
		01	RX (B) TX (D)
		10	RX (L) TX (D)
		11	RX (A) TX (D)
1	0	00	RX (D) TX (D)
		01	RX (D) TX (D)
		10	RX (D) TX (B)
		11	RX (D) TX (A)
1	1	00	RX (D) TX (D)
		01	RX (B) TX (D)
		10	RX (L) TX (B)
		11	RX (A) TX (A)

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8.14. Input and Output Drop Function

If some destination ports are blocking, or the buffer is full, the frames to these ports will be dropped.

There are two types of drop:

- Input Drop: Drop the frame directly. Do not forward to any port
- Output Drop: Forward only to non-blocking ports

For the RTL8309M, the dropping of broadcast, multicast, and unknown DA frames can be controlled independently.

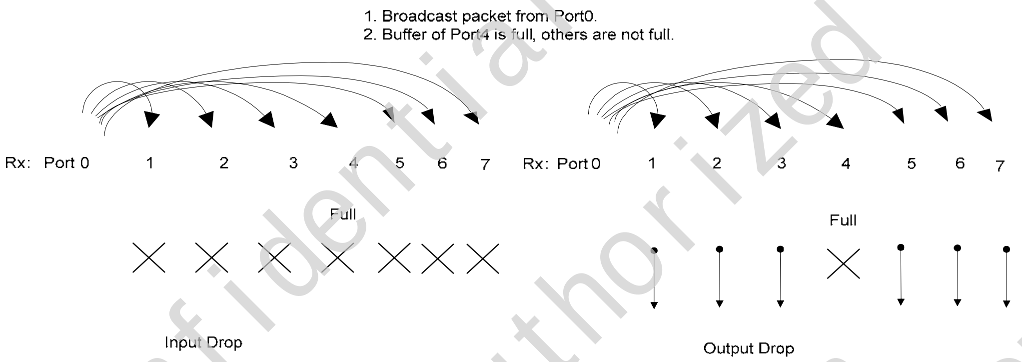

Figure 20. Broadcast Input Drop vs. Output Drop

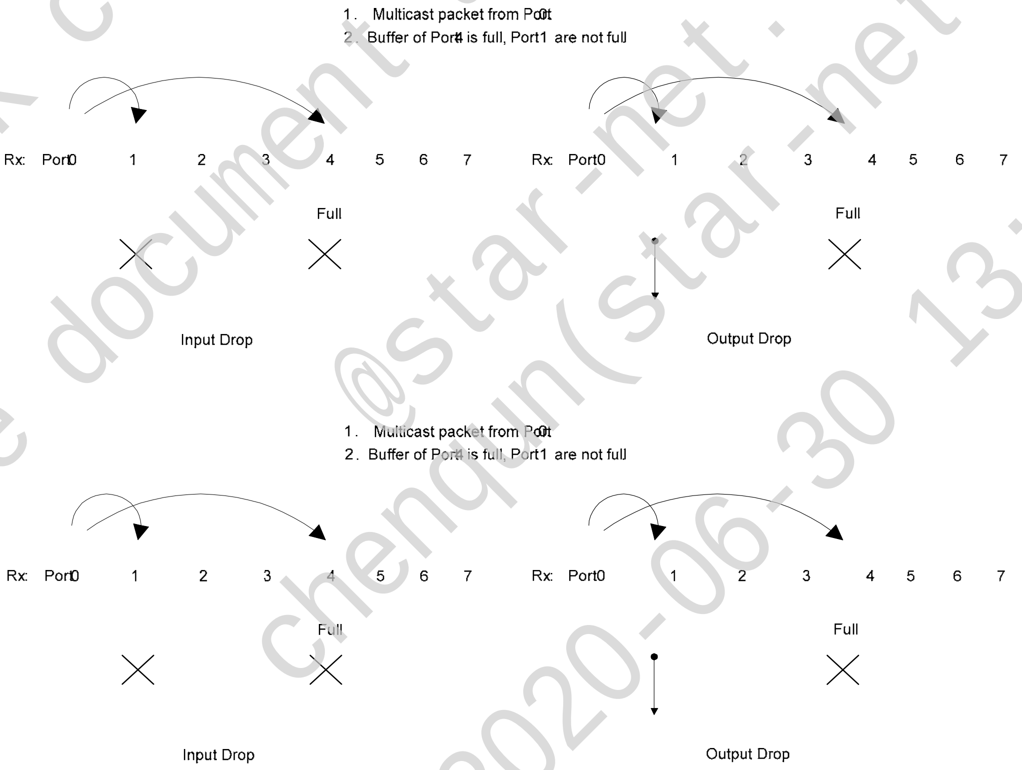

Figure 21. Multicast Input Drop vs. Output Drop

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8.15. Port Mirroring

The RTL8309M supports one set of mirroring functions for all 9 ports. The Mirror port can mirror both the TX and RX packets of the mirrored port. When a port is set as mirror port, mirrored packets will be sent to this port. Only one port can be set as mirror port. The mirror port can be selected in Mirror Port ID [3:0]. Mirror Port ID set to 0 to 8 corresponding to RTL8309M's port0 to port8. The mirrored TX port and the mirrored RX port can be selected in Enable mirror port [8:0] TX and Enable mirror port [8:0] RX. bit-0 to bit-8 in mirror port [8:0] TX/RX corresponding to port0 to port8.

Table 21. Bit to Mirror Port TX/RX Mapping

TX/RX MSB								LSB
Port 8	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1	Port 0

If the mirror port and normal port send packets to mirrored ports at the same time, and mirror self filter is enabled (Enable mirror filter=1), mirrored TX packets will not include packets sent from the mirror port. For example, Port_M mirror port_N TX, Port_N TX packets include packets from port_M and port_L. If Enable mirror filter=1, port_M can only mirror packets from port_L.

If the SA and DA filter function is enabled (Enable mirror function=1), the mirror port can only mirror a TX mirrored port's packets with a matching DA (depending on the Mirrored MAC address [47:0] register setting). The Mirror port can also only mirror an RX mirrored port's packets with a matching SA (depending on the Mirrored MAC address [47:0] register setting).

The mirror port also has the VLAN mirror leaky function. When mirrored ports belong to one VLAN (A), and the mirror port belongs to another VLAN (B), the mirror port can mirror packets inter-VLAN when Disable inter-VLANs mirror function=0.

If the mirror port is not validated, it cannot mirror other ports. If the mirror port has been validated, but the mirrored port TX is not validated, the mirror port can mirror RX, but cannot mirror TX.

If the CPU port is set as mirror port, mirrored packets will have a CPU tag (if CPU tag function is enabled). If the CPU port is set as mirrored port, the mirror port cannot mirror packets with a CPU tag, but can mirror packets without a CPU tag.

When mirroring TX, if one queue by which packets are sent out is full, the Mirror port cannot mirror TX, but can mirror RX.

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8.16. LED Function

The RTL8309M provides flexible LED functions for diagnostics. The LEDs can be configured to indicate the link information (link, activity, speed, duplex), and collision & loop detection information.

The parallel LED for each port indicates the port's link information when loop-detection is disabled or no loop condition occurs. If the loop is detected on a port, the parallel LED will blink.

All LED statuses are represented as active-low or high depending on input strapping.

LED_BLINK_TIME determines the LED blinking period for activity and collision via register (0: 32ms and 1: 128ms).

Some LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active high after reset. Otherwise, if the pin input is pulled high upon reset, the pin output is active low after reset.

Figure 22 shows example circuits for LEDs. Typical values for pull-down resistors are 10KΩ.

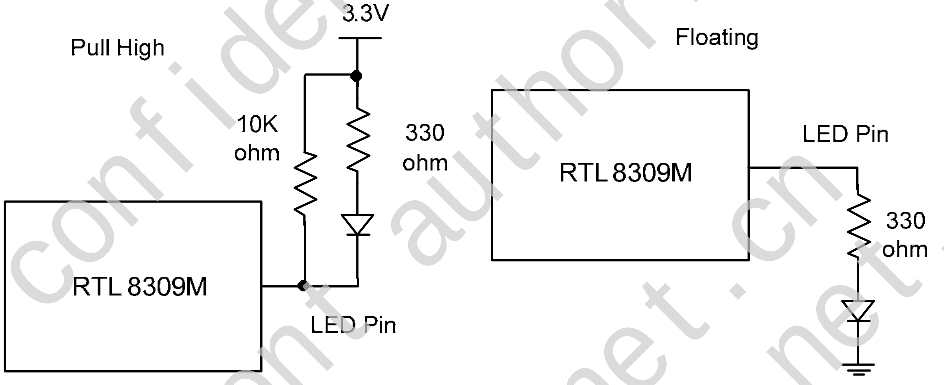

Figure 22. Floating and Pull-High of LED Pins for LED

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8.17. Energy-Efficient Ethernet (EEE)

The RTL8309M supports Energy-Efficient Ethernet (EEE) function as defined in IEEE 802.3az. The EEE function implements the Low Power Idle (LPI) mode at 100Mbps operation to save power during periods of low link utilization. In Low Power Idle mode, devices on both sides of the link disable portions of the functionality to lower the power consumption.

At the transmitter side, the RTL8309M port 0~7 can automatically enter or quit LPI mode based on their transmission loading. When a port's EEE function is enabled, the transmission loading is monitored in real time. If the transmission loading is lower than a preset threshold, this port's transmission circuit will enter LPI mode during the idle period. When there are packets to be transmitted, this port wakes up and quits LPI mode.

There are two types of wake-up:

- Packets in a high priority queue or a control packet (e.g., a PAUSE frame). These can wake up the port immediately
- Packet in a low priority queue that reach a preset number. A port in LPI mode can be woken up by low priority packets when the number of the cumulated low priority packets exceeds the preset threshold or a delay timer expires

At the receiver side, each embedded PHY of the RTL8309M will automatically respond to the request from the link partner to enter or quit the LPI mode.

The EEE ability for 100Base-TX on each side of a link should be exchanged via auto-negotiation. Auto-negotiation is mandatory when EEE is enabled. The MDIO Manageable Device (MMD), defined in IEEE 802.3, Clause 45, should also be supported, as the EEE register is located in the MMD of each PHY.

The RTL8309M also supports EEE at 10Mbps operation by reducing the transmit amplitude (10Base-Te). 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of Category 5 or better cable.

The EEE function for each port is enabled by default and can be disabled independently via strapping pin, registers, or EEPROM configurations.

8.18. Cable Diagnosis

The RTL8309M physical layer transceivers use DSP technology to implement the Realtek Cable Tester (RTCT) feature for cable diagnosis. The RTCT feature can detect short, open, or normal in both differential pair signal runs.

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9. Characteristics

9.1. Electrical Characteristics/Maximum Ratings

WARNING: Maximum ratings are limits beyond which permanent damage may be caused to the device or which may affect device reliability. All voltages are specified reference to GND unless otherwise specified.

Table 22. Electrical Characteristics/Maximum Ratings

Parameter	Min	Max	Units
DVDDH, AVDDH, AVDDHPLL Supply Referenced to GND	GND-0.3	+3.63	V
DVDDL, AVDDL, AVDDLPLL Supply Referenced to GND	GND-0.3	+1.10	V

9.2. Operating Range

Table 23. Operating Range

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Ambient Operating Temperature (Ta)	0	+70	°C
3.3V Vcc Supply Voltage Range (DVDDH, AVDDH, AVDDHPLL)	3.13	3.47	V
1.0V Vcc Supply Voltage Range (DVDDL, AVDDL, AVDDLPLL)	0.95	1.05	V

9.3. DC Characteristics

Table 24. DC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
TTL Input High Voltage	V_{ih}	-	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	-	0.8	V
TTL Input Current	I_{in}	-	-10	-	10	µA
TTL Input Capacitance	C_{in}	-	-	3	-	pF
Output High Voltage	V_{oh}	-	2.25	-	-	V
Output Low Voltage	V_{ol}	-	-	-	0.4	V
Output Three State Leakage Current	$\lvert I_{OZ} \rvert$	-	-	-	10	µA
Power Supply Current for 1.0V	Icc	10Base-T, idle 10Base-T, Peak continuous 100% utilization 100Base-TX, idle 100Base-TX, Peak continuous 100% utilization Link down	- - - - -	31 33 113 113 30	- - - - -	mA
Power Supply Current for 3.3V	Icc	10Base-T, idle 10Base-T, Peak continuous 100% utilization 100Base-TX, idle 100Base-TX, Peak continuous 100% utilization Link down	- - - - -	27 142 152 152 25	- - - - -	mA

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Parameter	SYM	Condition	Min	Typical	Max	Units
Total Power Consumption for All Ports	PS	10Base-T, idle	-	120.1	-	mW
		10Base-T, Peak continuous 100% utilization	-	502.6	-	
		100Base-TX, idle	-	613.6	-	
		100Base-TX, Peak continuous 100% utilization	-	615.6	-	
		Link down	-	112.5	-	

Note: All power supply currents are measured under the following conditions:
1. DVDDL=AVDDL=AVDDHPLL=1.0V; DVDDH=AVDDH=AVDDHPLL=3.3V.
2. Room temperature.
3. The EEE and Green features are disabled.
4. All LEDs are in low-active mode.
5. LDO power is not included.

9.4. Digital Timing Characteristics

9.4.1. (T)MII/RMII Interface Timing

9.4.1.1 MII MAC Mode Timing

Table 25. MII MAC Mode Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
100BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	I	40+100 ppm	40 ppm	40-100 ppm	ns
10BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	I	400+100 ppm	400 ppm	400-100 ppm	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Setup Time	T_{OS}	TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge setup time	O	15	-	-	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Hold Time	T_{OH}	TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge hold time	O	2	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Setup Time	T_{IS}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge setup time	I	4	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Hold Time	T_{IH}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge hold time	I	3	-	-	ns

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9.4.1.2 *MII PHY Mode Timing*

Table 26. MII PHY Mode Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
100BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	O	40+50 ppm	40 ppm	40-50 ppm	ns
10BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	O	400+50 ppm	400 ppm	400-50 ppm	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Setup Time	T_{OS}	TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge setup Time	O	15	-	-	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Hold Time	T_{OH}	TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge Hold Time	O	15	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Setup Time	T_{IS}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge setup time	I	10	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Hold Time	T_{IH}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge hold time	I	0	-	-	ns

9.4.1.3 *TMII MAC Mode Timing*

Table 27. TMII MAC Mode Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
100BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	I	20+100 ppm	20 ppm	20-100 ppm	ns
10BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	I	200+100 ppm	200 ppm	200-100 ppm	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Setup Time	T_{OS}	TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge setup time	O	7	-	-	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Hold Time	T_{OH}	TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge hold time	O	2	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Setup Time	T_{IS}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge setup time	I	4	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Hold Time	T_{IH}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge hold time	I	3	-	-	ns

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9.4.1.4 TMII PHY Mode Timing

Table 28. TMII PHY Mode Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
100BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	O	20+50 ppm	20 ppm	20-50 ppm	ns
10BaseT TXC/PRXC, RXC/PTXC	T_{cyc}	TXC/PRXC, RXC/PTXC clock cycle time	O	200+50 ppm	200 ppm	200-50 ppm	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Setup Time	T_{OS}	100BaseT TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge Setup Time	O	9	-	-	ns
TXD[3:0]/PRXD[3:0], TXEN/PRXDV Hold Time	T_{OH}	100BaseT TXD[3:0]/PRXD[3:0], TXEN/PRXDV to TXC/PRXC rising edge Hold Time	O	6	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Setup Time	T_{IS}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge setup time	I	6	-	-	ns
RXD[3:0]/PTXD[3:0], RXDV/PTXEN Hold Time	T_{IH}	RXD[3:0]/PTXD[3:0], RXDV/PTXEN to RXC/PTXC rising edge hold time	I	0	-	-	ns

9.4.1.5 RMII Timing

Table 29. RMII Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
REFCLK	T_{cyc}	REFCLK clock cycle time	I/O	20+50 ppm	20 ppm	20-50 ppm	ns
TXD[1:0], TXEN Setup Time	T_{OS}	TXD[1:0], TXEN to REFCLK rising edge setup time	O	4	-	-	ns
TXD[1:0], TXEN Hold Time	T_{OH}	TXD[1:0], TXEN to REFCLK rising edge hold time	O	2	-	-	ns
RXD[1:0],CRSDV Setup Time	T_{IS}	RXD[1:0], CRSDV to REFCLK rising edge setup time	I	4	-	-	ns
RXD[1:0], CRSDV Hold Time	T_{IH}	RXD[1:0], CRSDV to REFCLK rising edge hold time	I	2	-	-	ns

9.4.2. LED Timing

Table 30. LED Timing

Parameter	SYM	Condition	Min	Typical	Max	Units
LED On Time	tLEDon	LED Blinking to Indicate Link Information	32	-	128	ms
LED Off Time	tLEDoff	LED Blinking to Indicate Link Information	32	-	128	ms

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9.4.3. Reception/Transmission Data Timing of SMI Interface

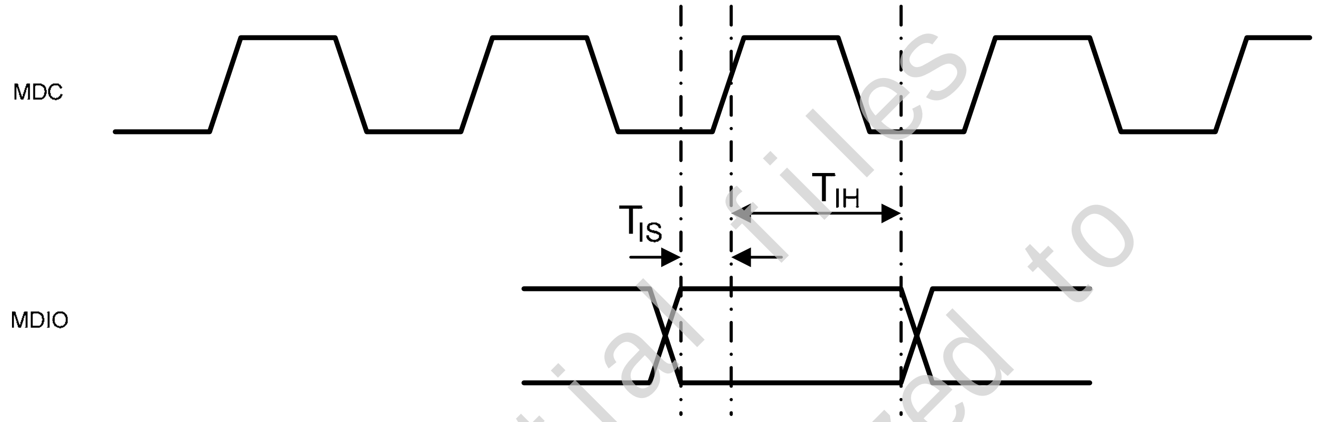

Figure 23. Reception Data Timing of SMI Interface

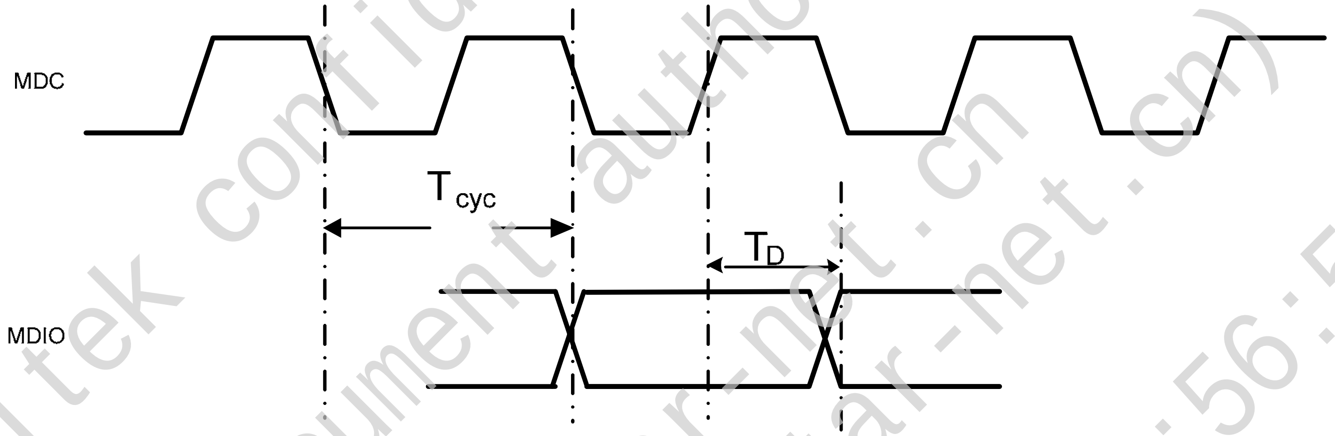

Figure 24. Transmission Data Timing of SMI Interface

Table 31. SMI Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
MDC	T_{cyc}	MDC Clock Cycle	I	400	-	-	ns
MDIO Input Setup Time	T_{IS}	MDIO to MDC Rising Edge Setup Time	I	50	-	-	ns
MDIO Input Hold Time	T_{IH}	MDIO to MDC Rising Edge Hold Time	I	10	-	-	ns
MDIO Output Delay Time	T_D	MDIO to MDC Rising Edge Output Delay	O	2	-	10	ns

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9.4.4. EEPROM Auto-Load Timing

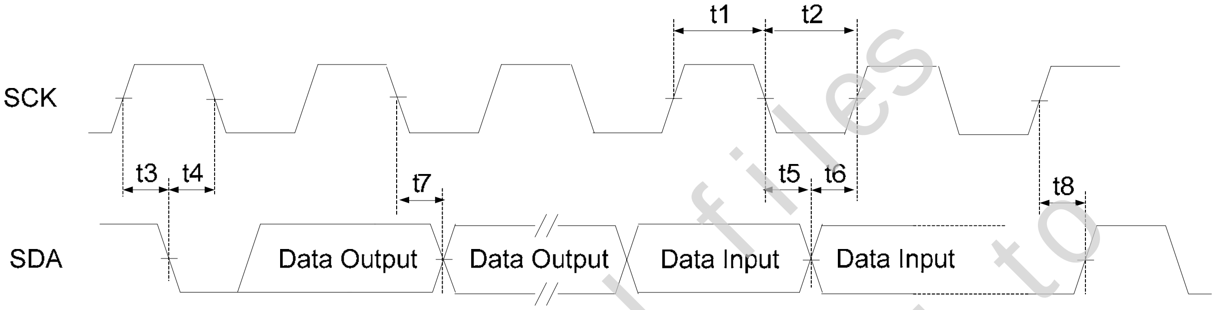

Figure 25. EEPROM Auto-Load Timing

Table 32. EEPROM Auto-Load Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
t1	SCL High Time	-	2.52	-	µs
t2	SCL Low Time	-	2.52	-	µs
t3	START Condition Setup Time	-	2.52	-	µs
t4	START Condition Hold Time	-	2.52	-	µs
t5	Data In Hold Time	0	-	-	ns
t6	Data In Setup Time	100	-	-	ns
t7	Data Output Hold Time	-	1.28	-	µs
t8	STOP Condition Setup Time	-	2.52	-	µs

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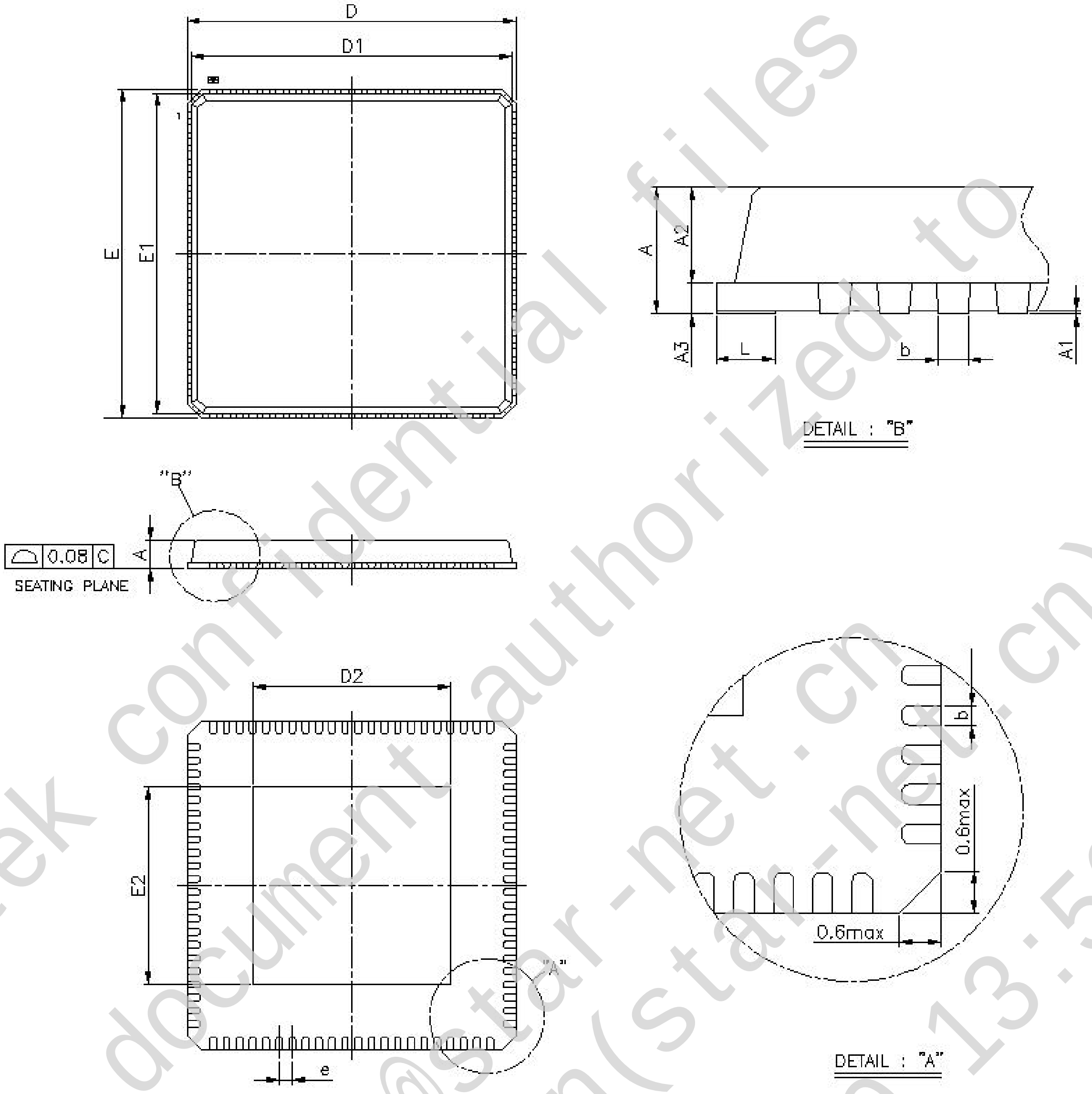
10. Mechanical Dimensions



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10.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	10.00BSC			0.394BSC		
D_1/E_1	9.75BSC	0.384BSC				
D_2/E_2	5.55	5.80	6.05	0.218	0.228	0.238
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 33. Ordering Information

Part Number	Package	Status
RTL8309M-CG	88-Pin QFN in 'Green' Package (RoHS Compliant)	MP

Note: See page 5 for package identification.

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